UMSDXXXGBP

Micro-SD 3.0 Memory Card Specification

Version 1.1

Revision History

Revision	History	Draft Date	Remark
1.0	First Release	2011-03-21	Andre
1.1	Mechanical Drawing updated	2011-07-01	Eric

A. General Description

The Micro Secure Digital (Micro SD) card version 3.0 is fully compliant to the specification released by SD Card Association. The Command List supports [Part 1 Physical Layer Specification Ver3.1 Final] definitions. Card Capacity of Non-secure Area, Secure Area Supports [Part 3 Security Specification Ver3.0 Final] Specifications.

The Micro-SD 3.0 card is based on 8-pin interface, designed to operate at a maximum operating frequency of 50MHz or 100MHz. It can alternate communication protocol between the SD mode and SPI mode. It performs data error detection and correction with very low power consumption.

Micro Secure Digital 3.0 card is one of the most popular cards today based on its high performance, good reliability and wide compatibility.

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B. Features

- Support SD system specification version 2.0 and 3.0.
- Card Capacity of Non-secure Area, Secure Area Supports [Part 3 Security Specification Ver3.1 Final] Specifications
- Support SD SPI mode
- Designed for read-only and read/write cards.
- Default mode : Variable clock rate 0-25MHz, up to 12.5MB/sec interface speed
- High-Speed mode : Variable clock rate 0-50MHz, up to 25MB/sec interface speed
- The Command List supports [Part 1 Physical Layer Specification Ver3.1 Final] definitions
- Copyrights Protection Mechanism - Complies with highest security of SDMI standard
- Password Protection of cards (option)
- Built-in write protection features (permanent and temporary)]
- High transmission speed
- +4KV/-4KV ESD protection in contact pads.
- Dimension : 15mm(L) x 11mm(W) x 1mm(H)

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C. Comparison of SD Card

	SD3.0 Standard (Backward compatible to 2.0 host)	SD3.0 SDHC (Backward compatible to 2.0 host)
Addressing Mode	Byte (1 byte unit)	Block (512 byte unit)
HCS/CCS bits of ACMD41	Support	Support
CMD8 (SEND_IF_COND)	Support	Support
CMD16 (SET_BLOCKLEN)	Support	Support (Only CMD42)
Partial Read	Support	Not Support
Lock/Unlock Function	Mandatory	Mandatory
Write Protect Groups	Optional	Not Support
Supply Voltage 2.0v – 2.7v (for initialization)	Not Support	Not Support
Total Bus Capacitance for each signal line	40pF	40pF
CSD Version (CSD_STRUCTURE Value)	1.0 (0x0)	2.0 (0x1)
Speed Class	Optional	Mandatory (Class 2/4/6/10)

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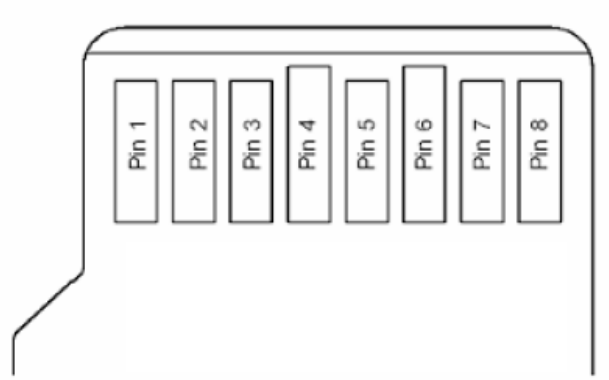
D. Pin Assignment



pin	SD Mode			SPI Mode		
	Name	Type[1]	Description	Name	Type	Description
1	DAT2	I/O/PP	Data Line[bit2]	RSV		
2	CD/DAT3 [2]	I/O/PP [3]	Card Detect/ Data Line[bit3]	CS	I [3]	Chip Select (neg true)
3	CMD	PP	Command/Response	DI	I	Data In
4	V_{DD}	S	Supply voltage	V_{DD}	S	Supply voltage
5	CLK	I	Clock	SCLK	I	Clock
6	V_{SS}	S	Supply voltage ground	V_{SS}	S	Supply voltage ground
7	DAT0	I/O/PP	Data Line[bit0]	DO	O/PP	Data Out
8	DAT1	I/O/PP	Data Line[bit1]	RSV		

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(1) S: power supply, I: input; O: output using push-pull drivers; PP: I/O using push-pull drivers

(2) The extended DAT lines (DAT1-DAT3) are input on power up. They start to operate as DAT lines after SET_BUS_WIDTH command. The Host shall keep its own DAT1-DAT3 lines in input mode, as well, while they are not used. It is defined so, in order to keep compatibility to Multimedia Cards.

(3) At power up this line has a 50KOhm pull up enabled in the card. This resistor serves two functions Card detection and Mode Selection. For Mode Selection, the host can drive the line high or let it be pulled high to select SD mode. If the host wants to select SPI mode it should drive the line low. For Card detection, the host detects that the line is pulled high. This pull-up should be disconnected by the user during regular data transfer period , with SET_CLR_CARD_DETECT(ACMD42) command.

Name	Width	Description
CID	128bit	Card identification number; card individual number for identification. **Mandatory**
RCA1	16bit	Relative card address; local system address of a card, dynamically suggested by the card and approved by the host during initialization. **Mandatory**
DSR	16bit	Driver Stage Register; to configure the card's output drivers. **Optional**
CSD	128bit	Card Specific Data; information about the card operation conditions. **Mandatory**
SCR	64bit	SD Configuration Register; information about the SD Memory Card's Special Features capabilities **Mandatory**
OCR	32bit	Operation conditions register. **Mandatory.**
SSR	512bit	SD Status; information about the card proprietary features **Mandatory**
OCR	32bit	Card Status; information about the card status **Mandatory**

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E. Power Consumption

Table list as below is the power consumption of SD card with different type of flash memory.

Flash mode	Max Power up Current (uA)	Max Stand by Current (uA)	Max Read Current (mA)	Max Write Current (mA)
Single(1) flash(1x8bit)	150	150	100@ 3.6V	100@ 3.6V

(1)Data transfer mode is single channel.

F. Electrical Specifications

Absolute Maximum Rating

Item	Symbol	Parameter	MIN	MAX	Unit
1	V_{DD}-V_{SS}	DC Power Supply	-0.3	+3.3	V
2	V_{IN}	Input Voltage	V_{SS}-0.3	V_{DD}+0.3	V
3	Ta	Operating Temperature	0	+70	℃
4	Tst	Storage Temperature	-25	+85	℃

Parameter	Symbol	Min	MAX	Unit
Operating Temperature	T_a	0	+70	℃
V_{DD} Voltage	V_{DD}	2.7	3.6	V

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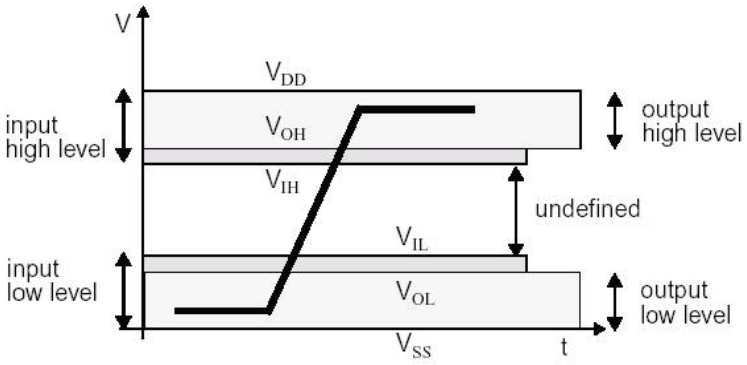
G. DC Characteristic

- **Threshold level for High Voltage Range**

Parameter	Symbol	Min	Max	Unit	Remarks
Supply voltage	V_{DD}	2.7	3.6	V	
Output High Voltage	V_{OH}	0.75*V_{DD}		V	IOH=-100uA V_{DD}Min.
Output Low Voltage	V_{OL}		0.125*V_{DD}	V	I_{OL} = 100uA $V_{DD\ min}$
Input High Voltage	V_{IH}	0.625*V_{DD}	V_{DD}+0.3	V	
Input Low Voltage	V_{IL}	V_{SS}-0.3	0.25 *V_{DD}	V	
Power up time			250	ms	from 0v to VDD min.

Bus Signal Levels



Bus signal levels

- **General**

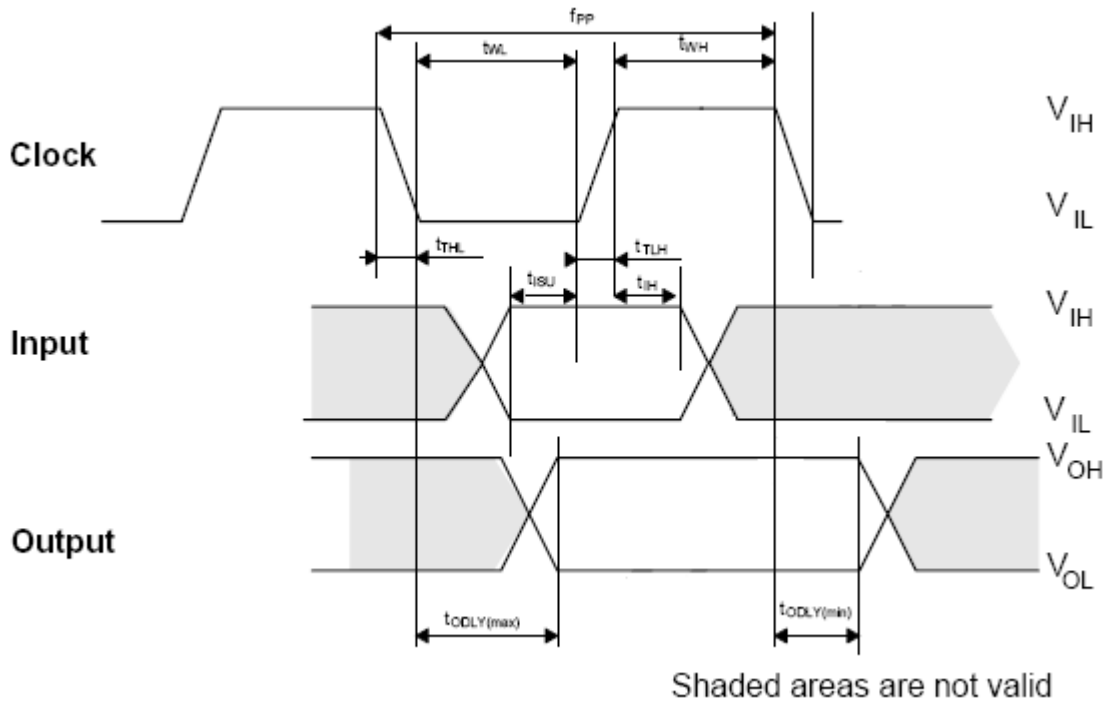
Parameter	Symbol	Min	Max.	Unit	Remarks
Peak voltage on all lines		-0.3	V_{DD}+0.3	V	
All Inputs					
Input Leakage Current		-10	10	uA	
All Outputs					
Output Leakage Current		-10	10	uA	

- **Bus Signal Line Levels**

Parameter	symbol	Min	Max	Unit	Remark
Pull-up resistance	R_{CMD} R_{DAT}	10	100	kΩ	to prevent bus floating
Total bus capacitance for each signal line	C_L		40	pF	1 card $C_{HOST}+C_{BUS}$ shall not exceed 30 pF
Capacitance of the card for each signal pin	C_{CARD}		10	pF	
Maximum signal line inductance			16	nH	f_{pp}<20 MHz
Pull-up resistance inside card (pin1)	R_{DAT3}	10	90	kΩ	May be used for card detection

H. AC Characteristic

H1. Micro SD Interface timing (Default)



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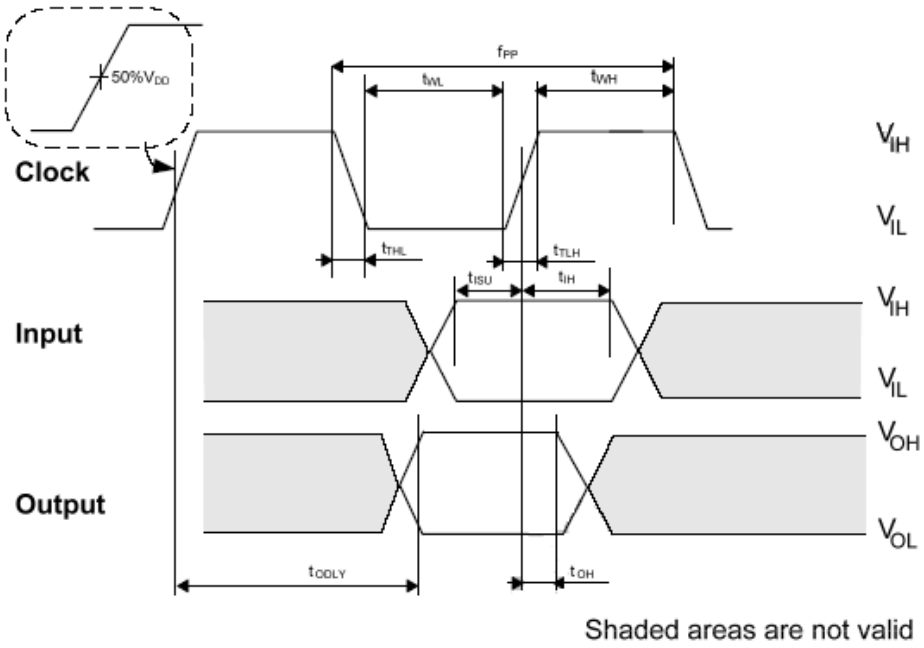
Parameter	Symbol	Min	Max	Unit	Remark
Clock CLK (All values are referred to min(V_{IH}) and max(V_{IL})					
Clock frequency Data Transfer Mode	f_{PP}	0	25	MHz	C_{card}≤□10 pF (1 card)
Clock frequency Identification Mode	f_{OD}	$0_{(1)}$/100	400	kHz	C_{card}≤□10 pF (1 card)
Clock low time	t_{WL}	10		ns	C_{card}≤□10 pF (1 card)
Clock high time	t_{WH}	10		ns	C_{card}≤□10 pF (1 card)
Clock rise time	t_{TLH}		10	ns	C_{card}≤□10 pF (1 card)
Clock fall time	t_{THL}		10	ns	C_{card}≤□10 pF (1 card)
Inputs CMD, DAT (referenced to CLK)					
Input set-up time	t_{ISU}	5		ns	C_{card}≤□10 pF (1 card)
Input hold time	t_{IH}	5		ns	C_{card}≤□10 pF (1 card)
Outputs CMD, DAT (referenced to CLK)					
Output Delay time during Data Transfer Mode	t_{ODLY}	0	14	ns	C_L≤40 pF (1 card)
Output Delay time during Identification Mode	tODLY	0	50	ns	C_L≤40 pF (1 card)

(1) 0Hz means to stop the clock. The given minimum frequency range is for cases were continues clock is required.

H2. Micro SD Interface timing (High-speed Mode)



Parameter	Symbol	Min	Max	Unit	Remark
Clock CLK (All values are referred to min(V_{IH}) and max(V_{IL})					
Clock frequency Data Transfer Mode	f_{PP}	0	50	MHz	C_{card}≤□10 pF (1 card)
Clock low time	t_{WL}	7		ns	C_{card}≤□10 pF (1 card)
Clock high time	t_{WH}	7		ns	C_{card}≤□10 pF (1 card)
Clock rise time	t_{TLH}		3	ns	C_{card}≤□10 pF (1 card)
Clock fall time	t_{THL}		3	ns	C_{card}≤□10 pF (1 card)
Inputs CMD, DAT (referenced to CLK)					
Input set-up time	t_{ISU}	6		ns	C_{card}≤□10 pF (1 card)
Input hold time	t_{IH}	2		ns	C_{card}≤□10

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					pF (1 card)
Outputs CMD, DAT (referenced to CLK)					
Output Delay time during Data Transfer Mode	t_{ODLY}		14	ns	C_L≤40 pF (1 card)
Output Hold time	T_{OH}	2.5	50	ns	C_L≤15 pF (1 card)
Total System capacitance of each line[1]	C_L		40	pF	CL≤15 pF (1 card)

(1) In order to satisfy severe timing, host shall drive only one card.

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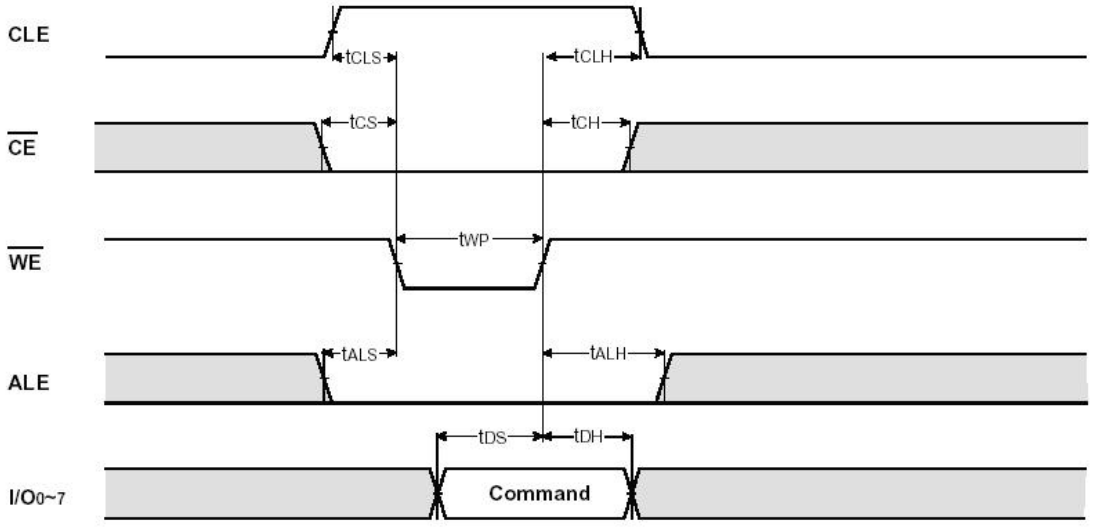
H3. Flash Interface AC Characteristic

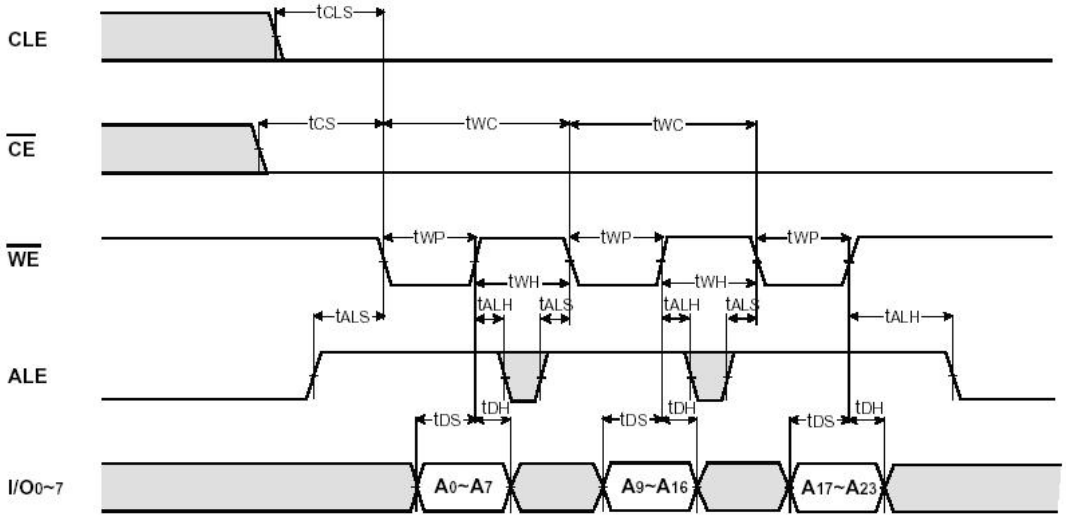
Parameter	Symbol	Min	Max	Unit
CLE Set-up Time	t_{CLS}	50	-	ns
CLE Hold Time	t_{CLH}	50	-	ns
/CE Setup Time	t_{CS}	200	-	ns
/CE Hold Time	t_{CH}	200	-	ns
WE Pulse Width	t_{WP}	30	50	ns
ALE Setup Time	t_{ALS}	50	-	ns
ALE Hold Time	t_{ALH}	50	-	ns
Data Setup Time	t_{DS}	20	50	ns
Data Hold Time	t_{DH}	30	100	ns
Write Cycle Time	t_{WC}	50	200	ns
WE High Hold Time	t_{WH}	20	150	ns
Read Cycle Time	t_{RC}	50	-	ns
/RE Pulse Width	t_{RP}	30	-	ns
/RE High Hold Time	t_{REH}	20	-	ns
Ready to /RE Low	t_{RR}	30	-	ns

H4. Flash memory timing

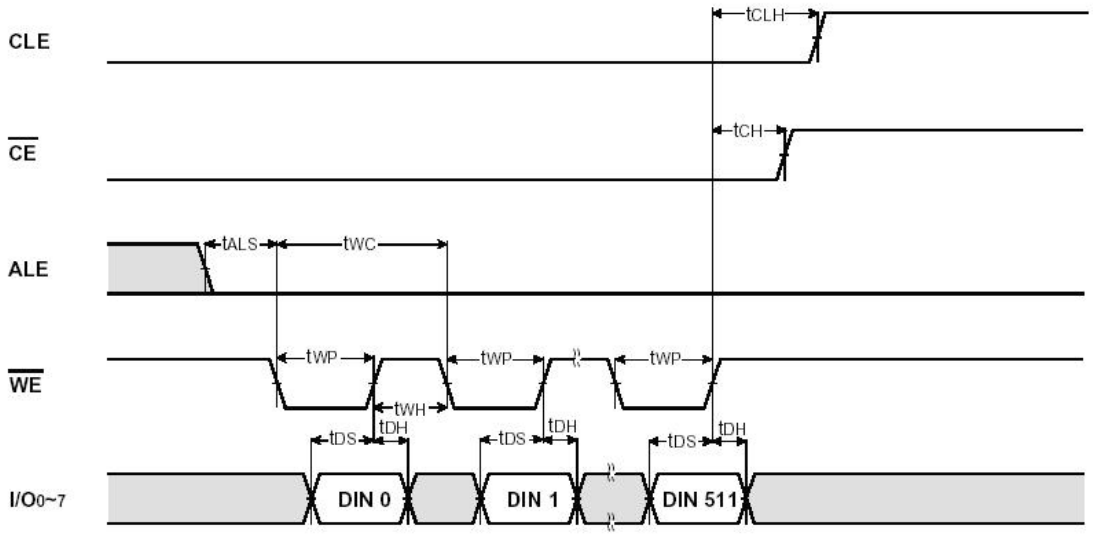
(a) Command Latch Cycle



(b) Address Latch Cycle



(c) Input Data Latch Cycle



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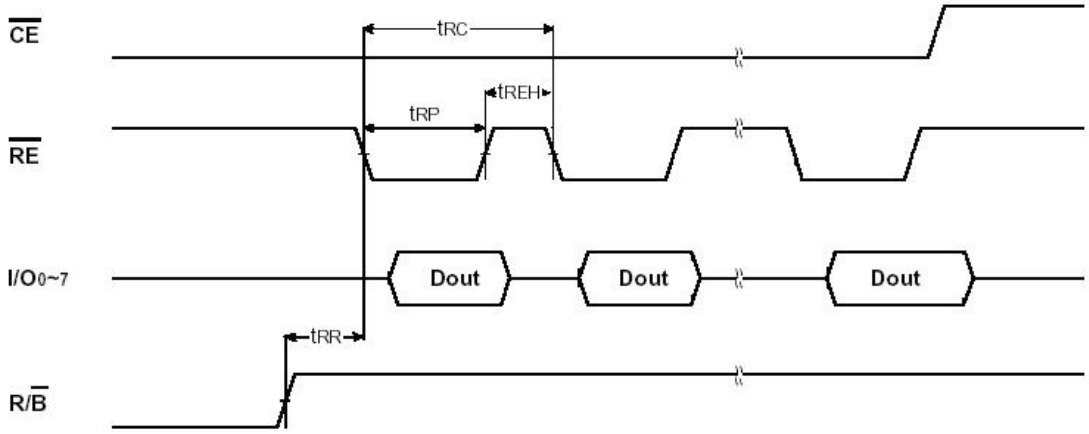
(d) Sequential Out Cycle after Read (CLE=L, /WE=H, ALE=L)



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I. Part Numbers

Part Number	Description	Operating Temperature
UMSD002GBP	2GB µSD	0°C ~ 70°C
UMSD004GBP	4GB µSD	0°C ~ 70°C
UMSD008GBP	8GB µSD	0°C ~ 70°C
UMSD016GBP	16GB µSD	0°C ~ 70°C
UMSD032GBP	32GB µSD	0°C ~ 70°C

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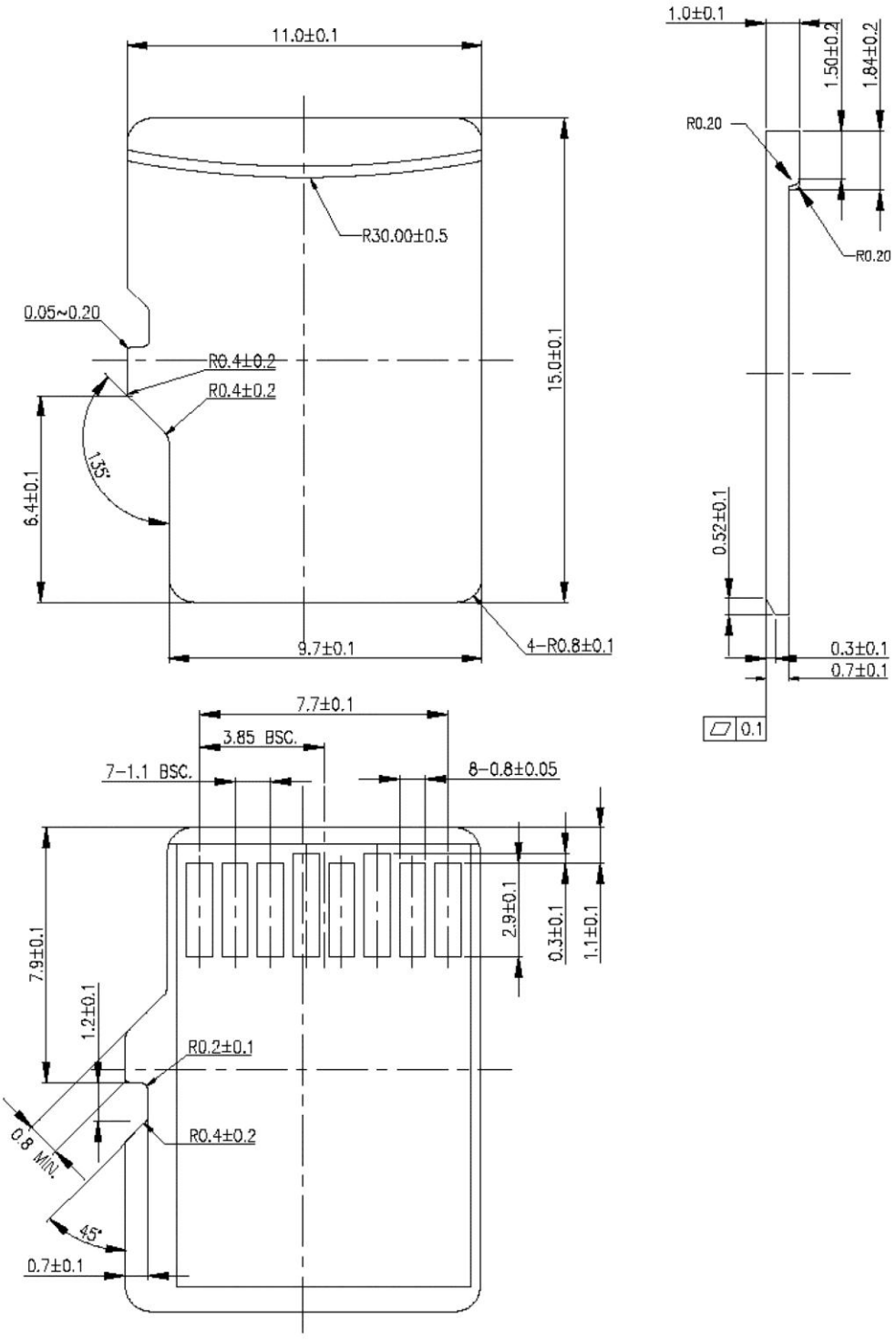
J. Dimension



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