Unity Digital
E Series(SLC Only)
2.5inch
IDE/PATA eSSD
Datasheet Rev. A

1. Product Description

Integral 2.5inch IDE/PATA SSD is based on standard IDE/ATA interface. It uses SLC or MLC NAND Flash and capacity can up to 128GB (SLC = E Series) and 256GB (MLC = Z Series).

2. Features

- Interface: IDE/PATA 50pin (44-pins IDE with gap and 4 jumper pins)
- Fully Compliant with ATA/ATAPI-7 Standard
- Capacities:

Item	Mechanical Height	Capacities
2.5inch (SLC)	9.3mm	8GB, 16GB, 32GB, 64GB, 128GB
2.5inch (MLC)	9.3mm	8GB, 16GB, 32GB, 64GB, 128GB, 256GB

- Performance

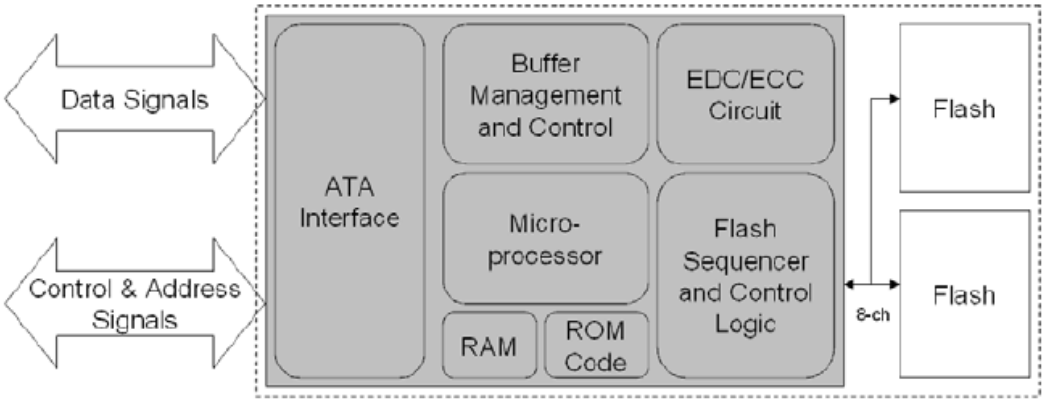
item	Read	Write	Random Read	Random Write
2.5inch (SLC)	88.1 MB/s	75.8 MB/s	82.1 MB/s	18.2 MB/s
2.5inch (MLC)	86.7 MB/s	69.8 MB/s	80.8 MB/s	16.9 MB/s

- Host Interface: 16-bit access
  - Support IDE PIO mode 0~4
  - Support IDE Multi-Word DMA mode 0~2
  - Support IDE Ultra DMA mode 0~5
- Low power, 5V Power Supply
- Low Current Operation:
  - Active mode: 410mA Typical
  - Sleep mode: 300µA Typical
- Support firmware ISP (in system programming) function, firmware upgradeable
- Supports SMART (Self-Monitor Analysis and Reporting Technology)
- Supports Dynamic and Static Wear Leveling
- Supports SLC and MLC NAND Flash
- Data integrity under power-cycling
- MTBF > 2,500,000 Hours
- High reliability based on internal BCH 15bit ECC
- Write Endurance
  - SLC: 100K cycles per block
  - MLC: 5K~10K cycles per block
- Data Retention
  - > 5 years (SLC)
- All non-Pb (lead-free) Devices are RoHS Compliant

3. Block Diagram

The following figure is the internal block diagram of Integral 2.5inch IDE/PATA eSSD

Figure 1: IDE/PATA eSSD Block Diagram



4. Pin assignments

Table 1 shows the pin configuration for IDE/PATA eSSD and Table 2 describes the pin descriptions for IDE/PATA

Table 1: IDE/PATA eSSD Pin Configuration

Pin No.	Name	Function	Pin No.	Name	Function
1	HRESET	Host Reset	2	GND	Ground
3	HDB[7]	Host Data Bit 7	4	HDB[8]	Host Data Bit 8
5	HDB[6]	Host Data Bit 6	6	HDB[9]	Host Data Bit 9
7	HDB[5]	Host Data Bit 5	8	HDB[10]	Host Data Bit 10
9	HDB[4]	Host Data Bit 4	10	HDB[11]	Host Data Bit 11
11	HDB[3]	Host Data Bit 3	12	HDB[12]	Host Data Bit 12
13	HDB[2]	Host Data Bit 2	14	HDB[13]	Host Data Bit 13
15	HDB[1]	Host Data Bit 1	16	HDB[14]	Host Data Bit 14
17	HDB[0]	Host Data Bit 0	18	HDB[15]	Host Data Bit 15
19	GND	Ground	20	KEY	Key-pin
21	DMARQ	DMA Request	22	GND	Ground
23	STOP[4]	Stop Ultra DMA burst	24	GND	Ground
25	HDMARDY	Ultra DMA ready	26	GND	Ground
	HSTROBE	Ultra DMA data strobe			
27	DDMARDY	Ultra DMA ready	28	CSEL	Master/Slave Select
	DSTROBE	Ultra DMA data strobe			
29	DMACK	DMA Acknowledge	30	GND	Ground
31	INTRQ	Interrupt Request	32	IOCS16	CS I/O 16-Bit
33	HAB[1]	Host Address Bit 1	34	PDIAG	Passed Diagnostic
35	HAB[0]	Host Address Bit 0	36	HAB[2]	Host Address Bit 2
37	CS0	Chip Select 0	38	CS1	Chip Select 1
39	DASP	Drive Active	40	GND	Ground
41	VCC	Supply Voltage	42	VCC	Supply Voltage
43	GND	Ground	44	NC	Not Connected
A	N/A	Master/Slave	B	N/A	Master/Slave

C	N/A	N/A	D	N/A	N/A

Table 2: IDE/PATA eSSD Pin Description

Pin Name	Pin No.	Description	I/O
Host side pins			
HRESET-	1	Host reset signal, High: Reset.	I
CS0-	37	Chip select CS0	I
CS1-	38	Chip select CS1	I
INTRQ	31	Host interrupt signal.	O
HDMARDY-	25	DMA ready during Ultra DMA data in burst	I
HSTROBE		Data strobe during Ultra DMA data out burst	
STOP	23	Stop during Ultra DMA data bursts	I
IOCS16-	32	Asserted in 16-bit access.	O
DDMARDY-	27	DMA ready during Ultra DMA data out burst	O
DSTROBE		Data strobe during Ultra DMA data in burst	
HDB[15:0]	18, 16, 14, 12, 10, 8, 6, 4, 3, 5, 7, 9, 11, 13, 15, 17	Host data bus	I/O
HAB[2:0]	33, 35, 36	Host Address bus	I/O
CSEL-	28	Master/Slave select signal (cable select signal). Low: Device operates as a master, High: Device operates as a slave.	I
DASP-	39	Used as an input port to check in the master mode to see if the slave is present or not, and as an output port to check in the slave mode to see if the slave for the master is present or not.	I/O
PDIAG-	34	Used as an input port to evaluate the result of slave diagnosis in the master mode, and as an output port to return the result of diagnosis to the master.	I/O
DMARQ	21	DMA Request.	O
DMACK-	29	DMA Acknowledge.	I
Power and Ground			
VCC	41, 42	Connect to VCC	VCC
GND	2, 19, 22, 24, 26, 30, 40, 43	Connect to GND.	GND
Other pins			
KEY	20	KEY Pin	N/A
Master/Slave	A, B	Set Master or Slave	I
NC	44, C, D	Not used. Please do not connect.	N/A

5. Specifications

5.1 CE and FCC Compatibility

IDE/PATA eSSD conforms to CE requirements and FCC standards

5.2 RoHS Compliance

IDE/PATA eSSD is fully compliant with RoHS directive.

5.3 Environment Specifications

5.3.1 Temperature

Table 3: Temperature Related Specifications

Item	Mode	Test Conditions
Standard	Operating	0 °C to +70 °C

Temperature	Non-operating	-45 °C to +85 °C
Humidity	Operating	5% to 95%, 20 °C
	Non-operating	5% to 95%, 30 °C

5.3.2 Shock and Vibration

Table 4: Shock and Vibration Specifications

Reliability	Mode	Test Conditions	Reference Standards
Vibration	Operating	7 Hz to 800 Hz, 2.15 G, 3 axes	IEC 68-2-6
	Non-operating	5 Hz to 500 Hz, 3.05 G, 3 axes	
Shock	Operating	Duration: 0.5 ms, 1,500 G, 3 axes	IEC 68-2-27
	Non-operating	Duration: 0.5 ms, 1,500 G, 3 axes	

5.3.3 Mean Time Between Failures (MTBF)

Table 5 summarizes the MTBF prediction results for various IDE/PATA eSSD configurations. The analysis was performed using a RAM CommanderTM failure rate prediction.

- Failure Rate: The total number of failures within an item population, divided by the total number of life units expended by that population, during a particular measurement interval under stated condition.
- Mean Time between Failures (MTBF): A basic measure of reliability for repairable items: The mean number of life units during which all parts of the item perform within their specified limits, during a particular measurement interval under stated conditions.

Table 5: IDE/PATA eSSD MTBF

Product	Condition	MTBF (Hours)	Failure Rate per Million Hours
2.5inch IDE/PATA eSSD	Telcordia SR-332 GB, 25°C	> 2,500,000	0.1938

5.4 General DC Characteristics

Table 6: DC Characteristics

I/O at 5.0V

Parameter	Symbol	Min.	Max.	Unit
Power Supply Voltage	V_{CC}	4.5	5.5	V
Input LOW Voltage	V_{IL}		0.6	V
Input HIGH Voltage	V_{IH}	4.0		V
Output LOW Voltage	V_{OL}		0.8	V
Output HIGH Voltage	V_{OH}	V_{CC} – 0.8		V
Pull up resistance	R_{PU}	50	73	KΩ
Pull down resistance	R_{PD}	50	97	KΩ

6 Timing Specifications

6.1 True IDE PIO Mode Read/Write Timing Specification

Figure 2: Read/Write Timing Diagram, PIO Mode

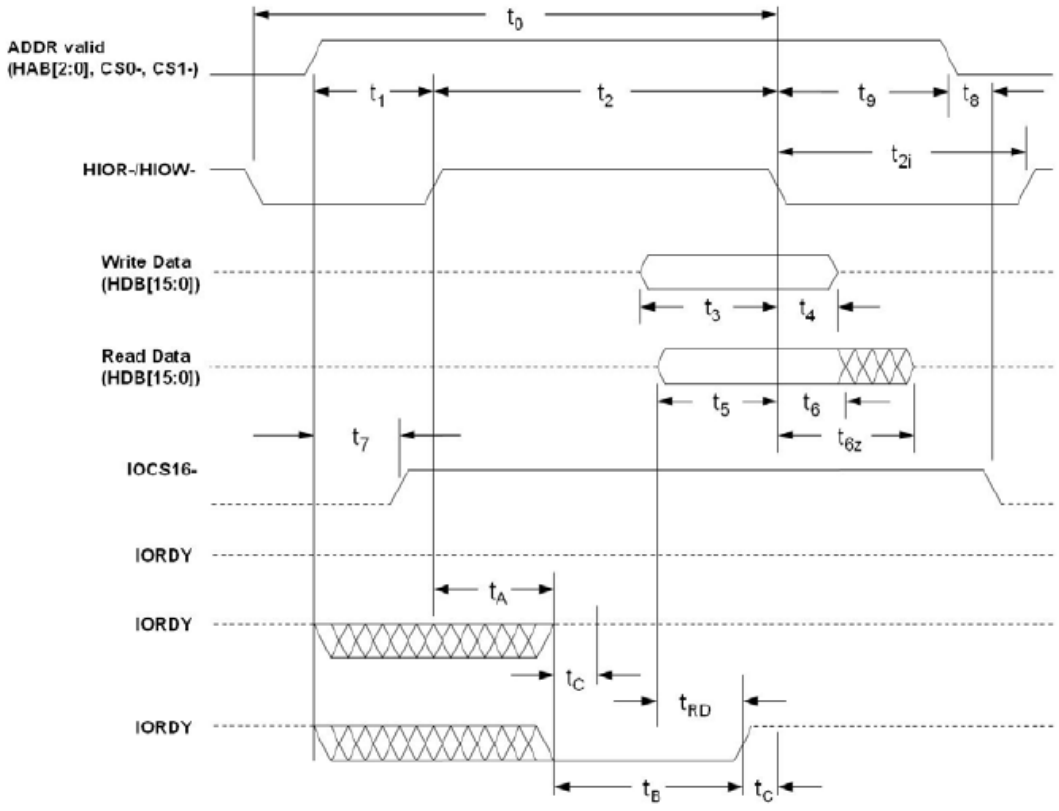


Table 7: Read/Write Timing Specifications, PIO Mode

PIO timing parameters		Mode 0	Mode 1	Mode 2	Mode 3	Mode 4
t_0	Cycle time (min.)	600	383	240	180	120
t_1	Address valid to HIOR-/HIOW- setup (min.)	70	50	30	30	25
t_2	HIOR-/HIOW- 16-bit (min.)	165	125	100	80	70
t_{2i}	HIOR-/HIOW- recovery time (min.)	-	-	-	70	25
t_3	HIOW- data setup (min.)	60	45	30	30	20
t_4	HIOW- data hold (min.)	30	20	15	10	10
t_5	HIOR- data setup (min.)	50	35	20	20	20
t_6	HIOR- data hold (min.)	5	5	5	5	5
t_{6z}	HIOR- data tri-state (max.)	30	30	30	30	30
t_7	Address valid to IOCS16- assertion (max.)	90	50	40	n/a	n/a
t_8	Address valid to IOCS16- released (max.)	60	45	30	n/a	n/a
t_9	HIOR-/HIOW- to address valid hold	20	15	10	10	10
t_{RD}	Read data valid to IORDY active (min.)	0	0	0	0	0
t_A	IORDY setup time	35	35	35	35	35
t_B	IORDY pulse width (max.)	1250	1250	1250	1250	1250
t_C	IORDY assertion to release (max.)	5	5	5	5	5

6.2 True IDE Multiword DMA Mode Read/Write Timing Specification

Figure 3: Read/Write Timing Diagram, Multiword DMA Mode

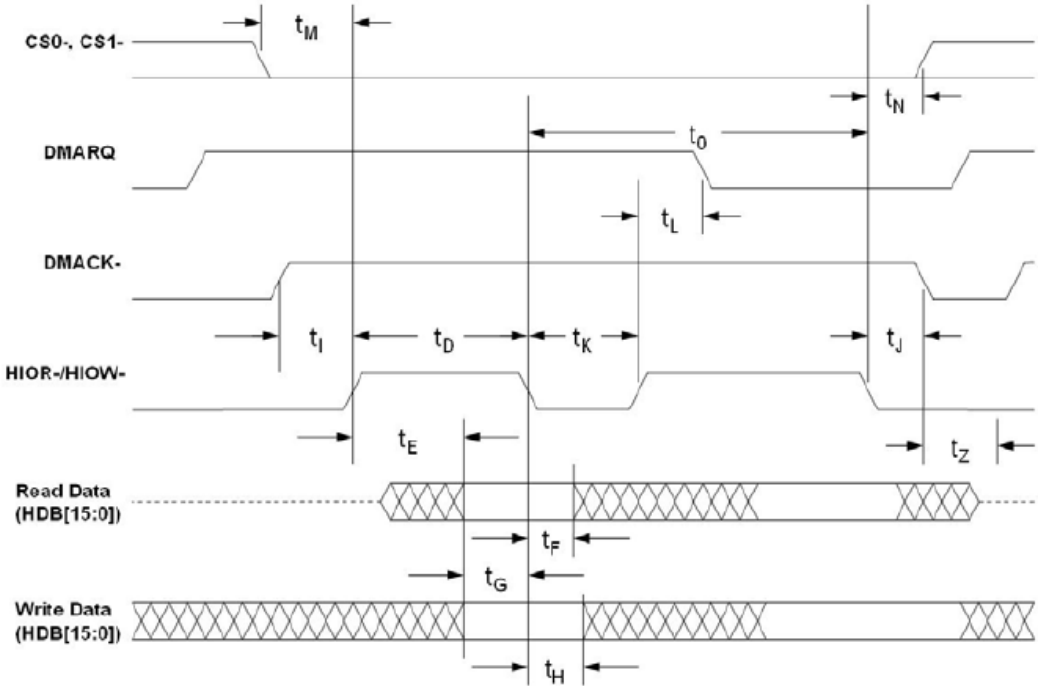


Table 8: Read/Write Timing Specifications, Multiword DMA Mode

Multiword DMA timing parameters		Mode 0	Mode 1	Mode 2
t_0	Cycle time (min.)	480	150	120
t_D	HIOR-/HIOW- assertion width (min.)	215	80	70
t_E	HIOR- data access (max.)	150	60	50
t_F	HIOR- data hold (min.)	5	5	5
t_G	HIOR-/HIOW- data setup (min.)	100	30	20
t_H	HIOW- data hold (min.)	20	15	10
t_I	DMACK to HIOR-/HIOW- setup (min.)	0	0	0
t_J	HIOR-/HIOW- to DMACK hold (min.)	20	5	5
t_{KR}	HIOR- negated width (min.)	50	50	25
t_{KW}	HIOW- negated width (min.)	215	50	25
t_{LR}	HIOR- to DMARQ delay (max.)	120	40	35
t_{LW}	HIOW- to DMARQ delay (max.)	40	40	35
t_M	CS1-, CS0- valid to HIOR-/HIOW-	50	30	25
t_N	CS1-, CS0- hold	15	10	10
t_Z	DMACK-	20	25	25

6.3 True IDE Ultra DMA Mode Read/Write Timing Specification

Figure 4: Ultra DMA Mode Data-in Burst Initiation Timing Diagram

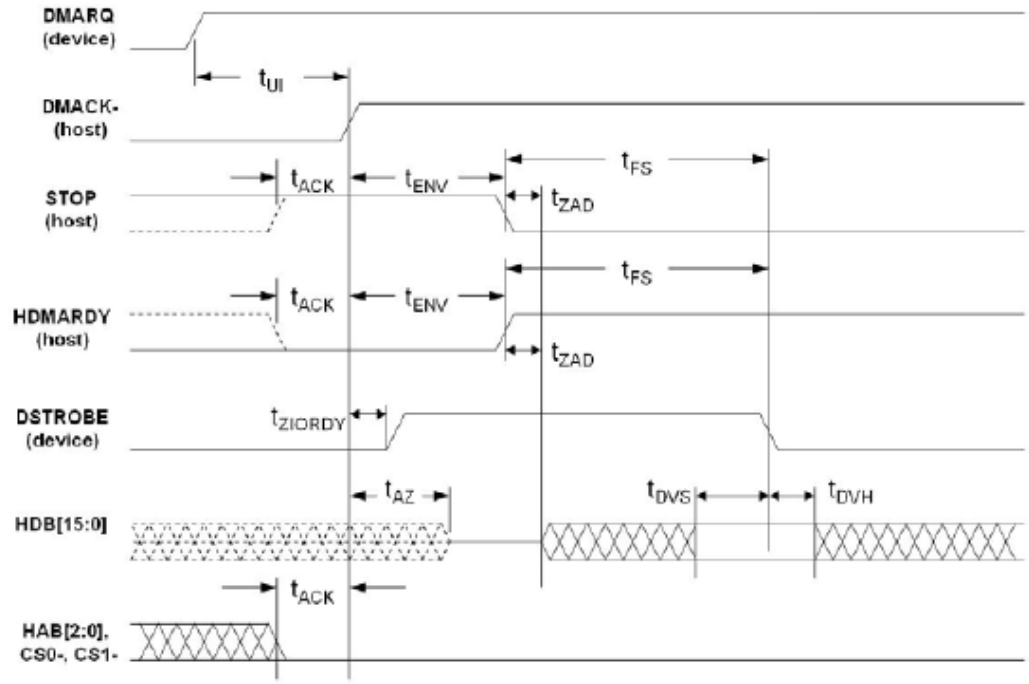


Figure 5: Ultra DMA Mode Data-out Burst Initiation Timing Diagram

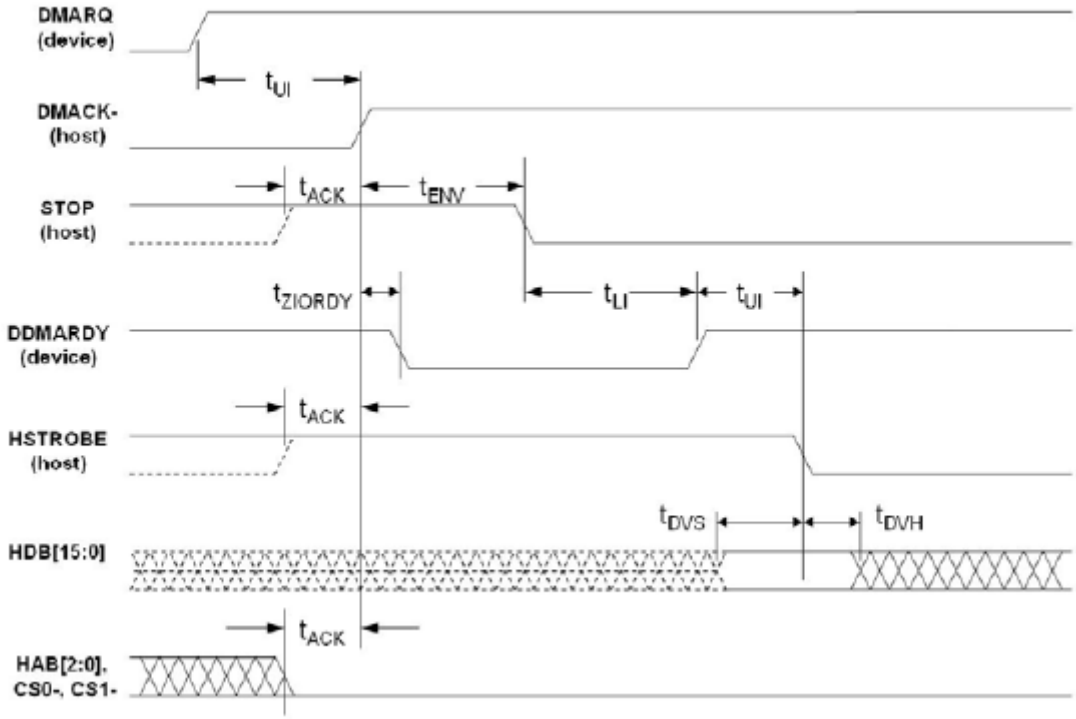


Figure 6: Sustained Ultra DMA Mode Data-in Burst Timing Diagram

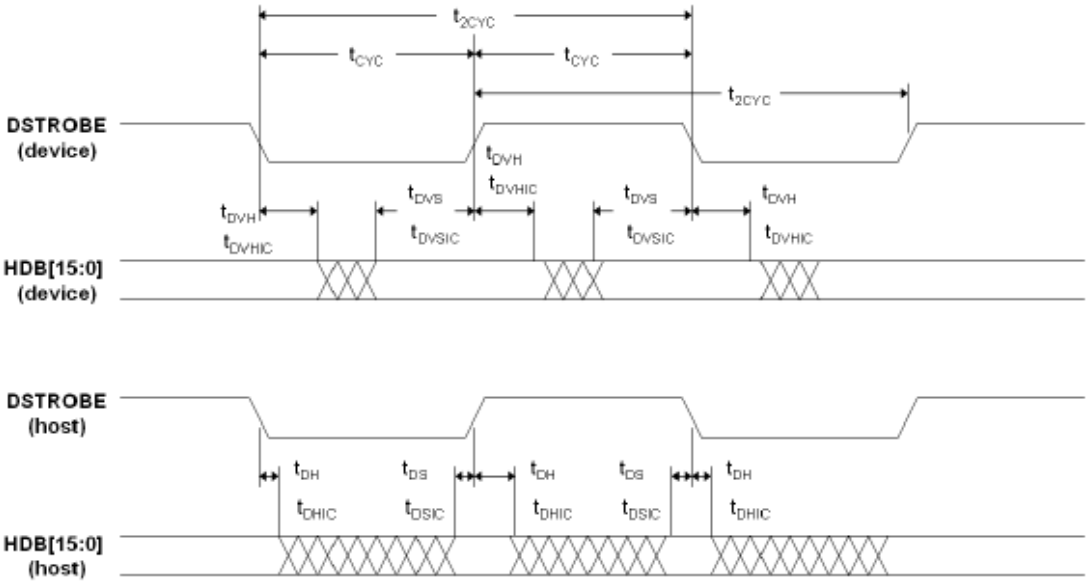


Figure 7: Sustained Ultra DMA Mode Data-out Burst Timing Diagram

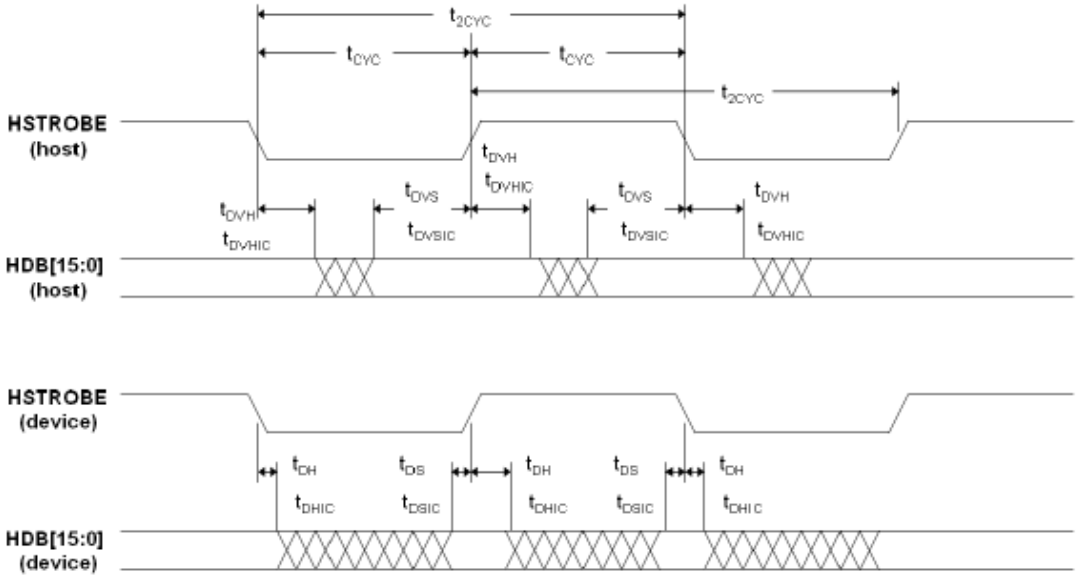


Table 9: Timing Diagram, Ultra DMA Mode

Ultra DMA timing parameters		Mode 0		Mode 1		Mode 2		Mode 3		Mode 4		Mode 5	
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.
t_{2CYC}	Typical sustained average two cycle time	240	-	160	-	120	-	90	-	60	-	40	-
t_{CYC}	Cycle time allowing for asymmetry and clock variations (from STROBE edge to STROBE edge)	112	-	73	-	54	-	39	-	25	-	16.8	-
t_{2CYC}	Two cycle time allowing for clock variations (from rising edge to next rising edge or from falling edge to next falling edge of STROBE)	230	-	153	-	115	-	86	-	57	-	38	-
t_{DS}	Data setup time (at recipient)	15	-	10	-	7	-	7	-	5	-	4	-
t_{DH}	Data hold time (at recipient)	5	-	5	-	5	-	5	-	5	-	4.6	-
t_{DVS}	Data valid setup time at sender (from data bus being valid until STROBE edge)	70	-	48	-	31	-	20	-	6.7	-	4.8	-

t_{DVH}	Data valid hold time at sender (from STROBE edge until data may become invalid)	6.2	-	6.2	-	6.2	-	6.2	-	6.2	-	4.8	-
t_{FS}	First STROBE time (for device to first negate DSTROBE from STOP during a data in burst)		230		200		170		130		120		90
t_{LI}	Limited interlock time	0	150	0	150	0	150	0	100	0	100	0	75
t_{MLI}	Interlock time with minimum	20	-	20	-	20	-	20	-	20	-	20	-
t_{UI}	Unlimited interlock time	0	-	0	-	0	-	0	-	0	-	0	-
t_{AZ}	Maximum time allowed for output drivers to release (from being asserted or negated)	-	10	-	10	-	10	-	10	-	10	-	10
t_{ZAH}	Minimum delay time required for output drivers to assert or negate (from released state)	20	-	20	-	20	-	20	-	20	-	20	-
t_{ZAD}		0	-	0	-	0	-	0	-	0	-	0	-
t_{ENV}	Envelope time (from DMACK- to STOP and HDMARDY- during data out burst initiation)	20	70	20	70	20	70	20	55	20	55	20	50
t_{RFS}	Ready-to-final-STROBE time (no STROBE edges shall be sent this long after negation of DMARDY-)	-	75	-	70	-	60	-	60	-	60	-	50
t_{RP}	Ready-to-pause time (time that recipient shall wait to initiate pause after negating DMARDY-)	160	-	125	-	100	-	100	-	100	-	85	-
t_{IORDYZ}	Pull-up time before allowing IORDY to be released	-	20	-	20	-	20	-	20	-	20	-	20
t_{ZIORDY}	Minimum time device shall wait before driving IORDY	0	-	0	-	0	-	0	-	0	-	0	-
t_{ACK}	Setup and hold times for DMACK- (before assertion or negation)	20	-	20	-	20	-	20	-	20	-	20	-
t_{SS}	Time from STROBE edge to negation of DMARQ or assertion of STOP (when sender terminates a burst)	50		50	-	50	-	50	-	50	-	50	-

7 Supported IDE Commands

IDE/PATA eSSD supports the commands listed in Table 11.

Table 11: IDE Commands

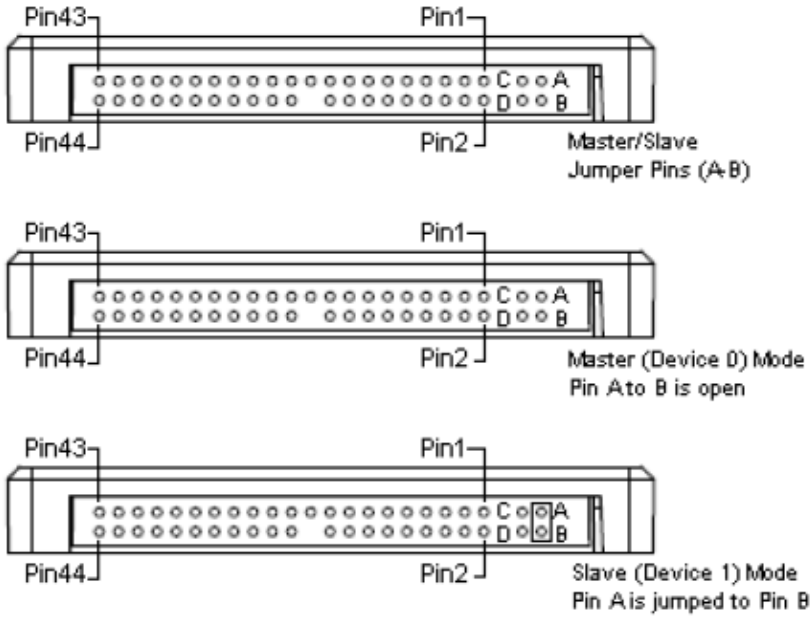
Command Name	Command Code
CHECK POWER MODE	98H or E5H
EXECUTE DEVICE DIAGNOSTIC	90H
ERASE SECTOR	C0H
FORMAT TRACK	50H
IDENTIFY DEVICE	ECH
IDLE	97H or E3H
IDLE IMMEDIATE	95H or E1H
INITIALIZE DRIVE PARAMETERS	91H
NOP	00H
READ BUFFER	E4H

READ DMA	C8H, C9H
READ MULTIPLE	C4H
READ SECTOR(S)	20H or 21H
READ VERIFY SECTOR(S)	40H or 41H
RECALIBRATE	1XH
REQUEST SENSE	03H
SECURITY DISABLE PASSWORD	F6H
SECURITY ERASE PREPARE	F3H
SECURITY ERASE UNIT	F4H
SECURITY FREEZE LOCK	F5H
SECURITY SET PASSWORD	F1H
SECURITY UNLOCK	F2H
SEEK	7XH
SET FEATURES	EFH
SET MULTIPLE MODE	C6H
SET SLEEP MODE	99H or E6H
STANDBY	96H or E2H
STANDBY IMMEDIATE	94H or E0H
TRANSLATE SECTOR	87H
WEAR LEVEL	F5H
WRITE BUFFER	E8H
WRITE DMA	CAH, CBH
WRITE MULTIPLE	C5H
WRITE MULTIPLE WITHOUT ERASE	CDH
WRITE SECTOR(S)	30H or 31H
WRITE SECTOR(S) WITHOUT ERASE	38H
WRITE VERIFY	3CH

8 Drive Configuration

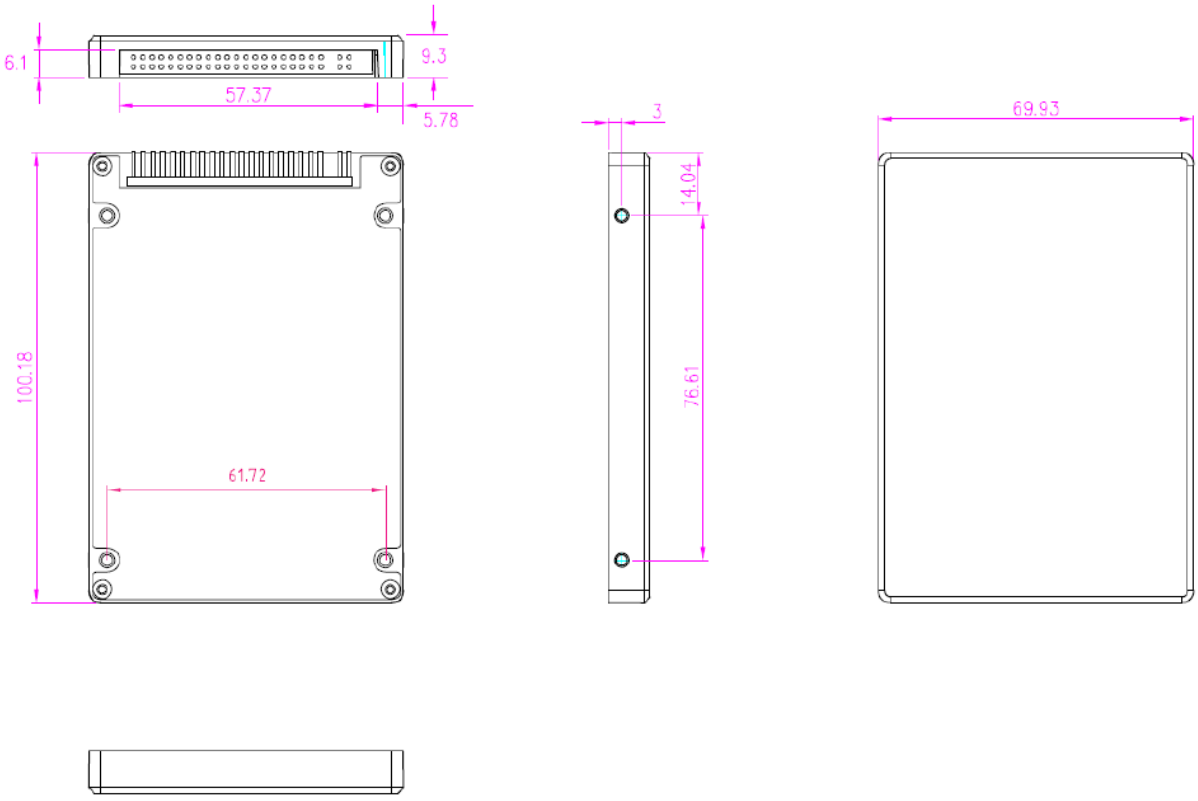
The drive must be configured to operate as either the Master (Device 0) or Slave (Device 1) IDE device. The Master /Slave setting represent the order of electronic devices on an IDE channel. If the SSD is the only PATA (IDE) drive installed in the system, the drive is configured as the master device. If two drives are installed in the machine, one device must be configured as the master and the remaining device as the slave. Jumper pins located at the rear of the SSD allow the user to configure the drive as either the master or the slave device.
To configure the SSD as either the Master or Slave device, place a jumper across the appropriate pins (A-B) as illustrated in follow figure.

Figure 8: Master and Slave Jumper Settings



9 Physical Dimensions

- 100.18 x 69.93 x 9.3mm



ORDERING INFORMATION:

PART NUMBER	DESCRIPTION
USSD008GBJEP	8GB SLC 2.5 inch PATA SSD
USSD016GBJEP	16GB SLC 2.5 inch PATA SSD
USSD032GBJEP	32GB SLC 2.5 inch PATA SSD
USSD064GBJEP	64GB SLC 2.5 inch PATA SSD
USSD128GBJEP	128GB SLC 2.5 inch PATA SSD