UNITY DIGITAL
USLF004/008/016/032/064SV+

GENERAL DESCRIPTON

Unity Digital's Flash Memory Card Series SV+ provides high density, high performance nonvolatile read/write solution for secure code storage, disk emulation, mobile PC and embedded applications. One of the key features of this card is that all data stored in the attribute memory is locked. The Series SV+ cards are built with Intel's 32/64/128Mb memory component JS28F320/640/128J3D with the manufacturer/device ID of $89/16_H/17_H/18_H$.

FEATURE

- Single Power Supply 3.3 – 5.0 V
- 250ns Maximum Access Time
- Up to 512 Independent Lockable Blocks
- 100,000 Erase Cycles per Block
- Conforms to PCMCIA Release 2.0
- PCMCIA Type II Form Factor

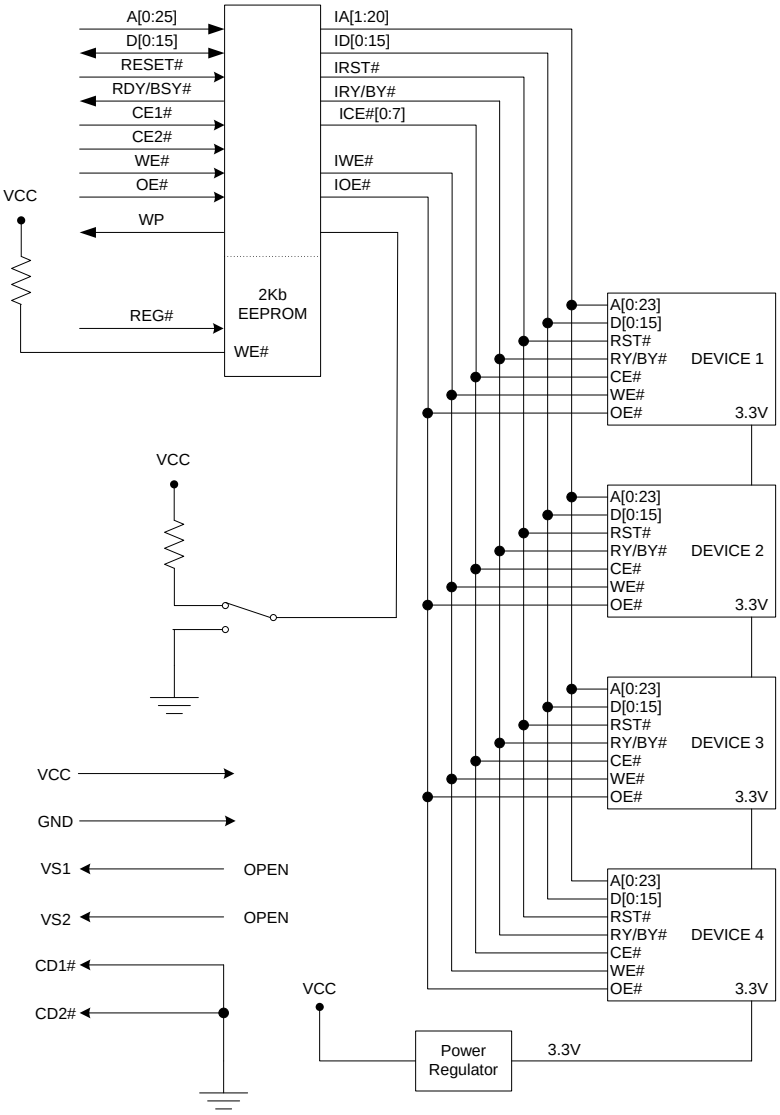
PIN ASSIGNMENT

Pin	Name	Function	Active	Pin	Name	Function	Active
1	GND	Ground		35	GND	Ground	
2	DQ_3	Data Bit 3		36	CD_1#	Card Detect 1	LOW
3	DQ_4	Data Bit 4		37	DQ_{11}	Data Bit 11	
4	DQ_5	Data Bit 5		38	DQ_{12}	Data Bit 12	
5	DQ_6	Data Bit 6		39	DQ_{13}	Data Bit 13	
6	DQ_7	Data Bit 7		40	DQ_{14}	Data Bit 14	
7	CE_1#	Card Enable 1	LOW	41	DQ_{15}	Data Bit 15	
8	A_{10}	Address Bit 10		42	CE_2#	Card Enable 2	LOW
9	OE#	Output Enable	LOW	43	VS_1#	Voltage Sense 1	
10	A_{11}	Address Bit 11		44	RFU	Reserved	
11	A_9	Address Bit 9		45	RFU	Reserved	
12	A_8	Address Bit 8		46	A_{17}	Address Bit 17	
13	A_{13}	Address Bit 13		47	A_{18}	Address bit 18	
14	A_{14}	Address Bit 14		48	A_{19}	Address Bit 19	
15	WE#	Write Enable	LOW	49	A_{20}	Address Bit 20	
16	RDY/BSY#	Ready Busy	LOW	50	A_{21}	Address Bit 21	
17	V_{CC}	Supply Voltage		51	V_{CC}	Supply Voltage	
18	V_{PP}	Program Voltage		52	V_{PP}	Program Voltage	
19	A_{16}	Address Bit 16		53	A_{22}	Address Bit 22	
20	A_{15}	Address Bit 15		54	A_{23}	Address Bit 23	
21	A_{12}	Address Bit 12		55	A_{24}	Address Bit 24	
22	A_7	Address Bit 7		56	A_{25}	Address Bit 25	
23	A_6	Address Bit 6		57	VS_2#	Voltage Sense 2	
24	A_5	Address Bit 5		58	RESET	Reset	HIGH
25	A_4	Address Bit 4		59	RFU	Reserved	
26	A_3	Address Bit 3		60	RFU	Reserved	
27	A_2	Address Bit 2		61	REG#	Attribute Memory Select	LOW
28	A_1	Address Bit 1		62	BVD_2	Battery Voltage Detect 2	
29	A_0	Address Bit 0		63	BVD_1	Battery Voltage Detect 1	
30	DQ_0	Data Bit 0		64	DQ_8	Data Bit 8	
31	DQ_1	Data Bit 1		65	DQ_9	Data Bit 9	
32	DQ_2	Data Bit 2		66	DQ_{10}	Data Bit 10	
33	WP	Write Protect	HIGH	68	CD_2#	Card Detect 2	LOW
34	GND	Ground		68	GND	Ground	

SIGNAL DESCRIPTION

Symbol	Type	Name and Function
$A_0 - A_{25}$	INPUT	**ADDRESS INPUTS:** Address A_0 through A_{25} are address bus lines which enable direct addressing of up to 64 megabytes of memory on the card. Signal A_0 is not used in word access mode. A_{25} is the most significant bit.
$DQ_0 - DQ_{15}$	INPUT/ OUTPUT	**DATA INPUT/OUTPUT:** DQ_0 through DQ_{15} constitute the bi-directional data bus. DQ_{15} is the most significant bit.
CE_1# - CE_2#	INPUT	**CARD ENABLE 1 & 2:** CE_1# enables even bytes. CE_2# enables odd bytes. Multiplexing A_0, CE_1#, and CE_2# allows 8-bit hosts to access all data on D_0 through D_7.
OE#	INPUT	**OUTPUT ENABLE:** Active low signal gating read data from the memory card.
RDY/BSY#	OUTPUT	**READY/BUSY OUTPT:** Indicates status of internally timed erase or write activities. A high output indicates the memory card is ready to accept access. A low output indicates that a device in the memory card is busy with internally timed erase or write activities.
CD_1#, CD_2#	OUTPUT	**CARD DETECT 1 &2:** These signals provide for correct memory card insertion detection. They are positioned at opposite ends of the card to detect proper alignment. The signals are connected to ground internally on the memory card, and will be force low whenever a card is placed in the socket. The host socket interface circuitry shall supply 10K or larger pull-up resistors on these signal pins.
WP	OUTPUT	**WRITE PROTECT:** Write Protect reflects the status of the Write Protect switch on the memory card. WP set to high = write protected, providing internal hardware write lockout to the flash array.
V_{PP}		**WRITE/ERASE POWER SUPPLY:**
V_{CC}		**CARD POWER SUPPLY:**
GND		**GROUND:** for all internal circuitry
REG#	INPUT	**REGISTER SELECT:** Provides access to Flash Memory Card register and Card Information Structure in the Attribute memory Plane.
RESET	INPUT	RESET: Active high signal for placing card in Power-On Default State.
BVD_1, BVD_2	OUTPUT	**BATTERY VOLTAGE DETECT:** These signals are driven high to maintain SRAM card compatibility
VS_1, VS_2	OUTPUT	**VOLTAGE SENSE:** Notify the host socket of the card's V_{CC} requirements. VS_1 and VS_2 open that indicate the available operation voltage is 5V only.
RFU		**RESERVE FOR FUTURE USE**
N.C.		**NO INTERNAL CONNECTION TO CARD:** Pin may be driven or left floating.

BLOCK DIAGRAM



FUNCTIONAL TRUE TABLE

COMMON MEMORY								
Mode	REG#	CE_2#	CE_1#	A_0	OE#	WE#	D[15:D8]	D[7:0]
Standby	X	H	H	X	X	X	HI-Z	HI-Z
Byte –Read	H	H	L	L	L	H	HI-Z	Even
	H	H	L	H	L	H	HI-Z	Odd
Word-Read	H	L	L	X	L	H	Odd	Even
Byte-Write	H	H	L	L	H	L	X	Even
	H	H	L	H	H	L	X	Odd
Word-Write	H	L	L	X	H	L	Odd	Even
ATTRIBUTE MEMORY								
Mode	REG#	CE_2#	CE_1#	A_0	OE#	WE#	D[15:D8]	D[7:0]
Standby	X	H	H	X	X	X	HI-Z	HI-Z
Byte –Read	L	H	L	X	L	H	HI-Z	Even
Word-Read	L	L	L	X	L	H	X	Even
Byte-Write	L	H	L	X	H	L	X	Even
Word-Write	L	L	L	X	H	L	X	Even

Notes: H: High L: Low
X: Don't care HI-Z: High Impedance

For details of information regarding the memory components modes of operation, commands, and programming, please consult the Intel Embedded Flash Memory (J3 v. D) Datasheet.

ASOLUTE MAXIMUM RATING*

Item	Symbol	Rating	Unit
Voltage on any pin relative to Vss	V_{IN}, V_{OUT}	-0.5 to 6.0	V
Voltage on Vcc supply relative to Vss	V_{CC}	-0.5 to 6.0	V
Storage Temperature	Tstg	-55 to 150	°C
Power Dissipation	Pd	8	W
Short Circuit Output Current	I_{OS}	50	mA

***** Stress greater than those list under "Absolute Maximum Rating" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED DC OPERATING CONDITION (Voltage referenced to V_{SS}, T_A = 0 to 70°C)

Item	Symbol	Min	Typ	Max	Unit	Notes
Supply Voltage	V_{CC}	3.0	3.3	5.5	V	
Ground	V_{SS}	0	0	0	V	
Input High Voltage	V_{IH}	2.0	-	V_{CC} + 0.3	V	1
Input Low Voltage	V_{IL}	-0.3	-	0.8	V	2

Notes:
1. V_{CC} + 1.3V at pulse width ≤ 15ns which is measured at V_{CC}.
2. –1.3V at pulse width ≤ 15ns which is measured at V_{SS}.

CIS for Series SV+ Card

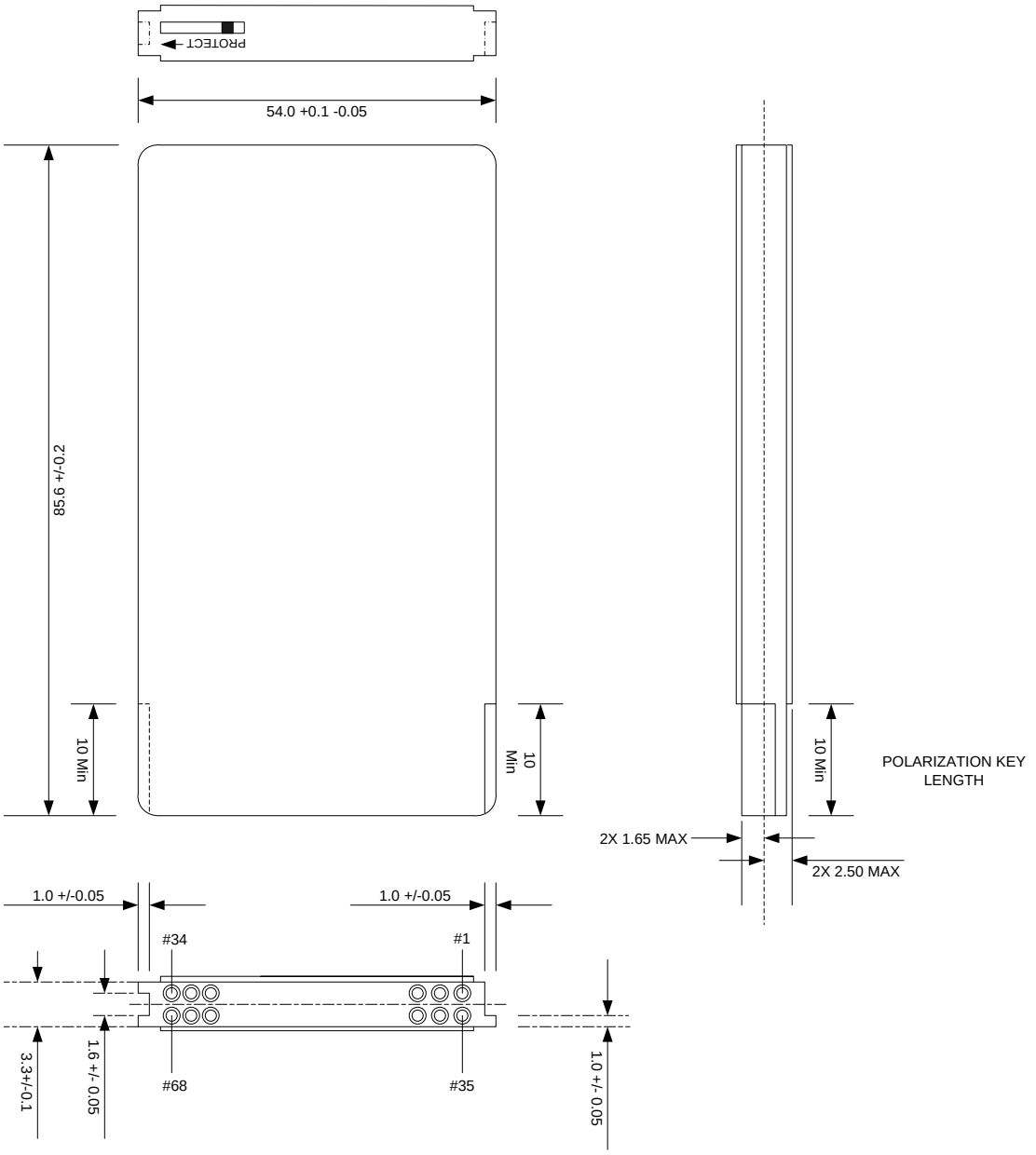
Address	Value	Description
00H	01H	Device Information
02H	03H	Tuple Link
04H	52H	FLASH = 200ns
06H		CARD SIZE
	0EH	4MB
	1EH	8MB
	3EH	16MB
	7EH	32MB
08H	FFH	End of Tuple
0AH	18H	JEDEC Code ID
0CH	03H	Tuple Link
0EH	89H	Manufacturer ID
10H		Device ID
	16H	32Mb
	17H	64Mb
	18H	128Mb
12H	FFH	End of Tuple
14H	1EH	Device Geometry
16H	07H	Tuple Link
18H	02H	Bus: 2 Bytes
1AH	11H	Erase Block: 64Kbytes
1CH	01H	Read Size: 1 Byte
1EH	01H	Write Size: 1 Byte
20H	01H	Partition: 1 Block
22H	01H	Non-Interleave
24H	FFH	End of Tuple
26H	15H	Version Information
28H	2CH	Tuple Link
2AH	04H	Major Version
2CH	01H	Minor Version
2EH	55H	U
30H	4EH	N
32H	49H	I
34H	54H	T
36H	59H	Y
38H	20H	SPACE
3AH	44H	D
3CH	49H	I
3EH	47H	G

Address	Value	Description
40H	49H	I
42H	54H	T
44H	41H	A
46H	4CH	L
48H	20H	SPACE
4AH	30H	0
	31H	1
	33H	3
4CH	32H	2
	34H	4
	36H	6
	38H	8
4EH	4DH	M
50h	42H	B
52H	20H	SPACE
54H	46H	F
56H	4CH	L
58H	41H	A
5AH	53H	S
5CH	48H	H
5EH	20H	SPACE
60H	43H	C
62H	11H	A
64H	52H	R
66H	44H	D
68H	20H	SPACE
6AH	53H	S
6CH	45H	E
6EH	52H	R
70H	49H	I
72H	45H	E
74H	53H	S
76H	20H	SPACE
78H	53H	S
7AH	56H	V
7CH	2BH	+
7EH	00H	End Text
80H	FFH	End of CIS

ORDERING INFORMATION:

CARD DENSITIES	UNITY DIGITAL PART NO.
4MB	USLF004 SV+
8MB	USLF008 SV+
16MB	USLF016 SV+
32MB	USLF032 SV+

CARD DIMENSION



UNIT: mm