Solid State Storage

PC Card
128MB - 8GB
Silver-1

General Description

Unity Digital's flash product adheres to the latest industry compliance and regulatory standards including UL, FCC, and RoHS. Each device incorporates a state-of-the-art flash memory controller that provides the greatest flexibility to customer applications while supporting key flash management features resulting in the industry's highest reliability and endurance. Key features:

- Built-in 4-symbol Reed-Solomon ECC engine detects and corrects errors
- Sophisticated block management and wear leveling algorithms dramatically enhance flash memory endurance
- Supports reliable high performance Single Level Cell (SLC) NAND flash technology
- Lifecycle management feature allows users to monitor the device's block management

Unity Digital's PC Card is for applications requiring high reliability and high tolerance to shock, vibration, humidity, altitude, ESD, and temperature. The rugged industrial design combined with temperature testing and adherence to rigid JEDEC JESD22 standards ensures flawless execution in the harshest environments. In addition to custom hardware and firmware designs, Unity Digital also offers value-added services:

- Custom labeling and packaging
- Custom software imaging and ID strings
- Full BOM control and product change notification

Storage Capacities:

128MB, 256MB, 512MB, 1GB, 2GB, 4GB, 8GB

Environment conditions:

- Commercial temperature: 0°C to 70°C
  Industrial temperature: -40°C to 85°C
  Storage temperature: -55°C to 125°C

ATA Compatibility:

- 3.3V or 5.0V single power supply
- 68 pin connector Type II form factor
- Support for CIS implementation with 256 bytes of attribute memory

Power consumption:

- 5V operation
  Active mode:
  Write operation: 28 mA (Typ.), 30 mA (Max.)
  Read operation: 23 mA (Typ.), 30 mA (Max.)
  Sleep mode: 2.0mA (max.)
- 3.3V operation
  Active mode:
  Write operation: 28 mA (Typ.), 30 mA (Max.)
  Read operation: 23 mA (Typ.), 30 mA (Max.)
  Sleep mode: 2.0mA (max.)

Interface modes

- PC card memory mode
- PC card I/O mode
- True IDE mode

High Performance

- Interface transfer speed in PIO mode 4 or MWDMA mode 2 cycle timing; up to 16.6MB/second (theoretical).
- Typical write: Up to 6.0 MBytes/s in ATA PIO mode 4
- Typical read: Up to 8.0 MBytes/s in ATA PIO mode 4
- On card ECC up to 6 Bytes per 512 Byte data sector

Dimensions: Type II form factor: 85.6mm(L) x 54.0mm(W) x 5.03mm(H)

MTBF > 4,000,000 hours

High shock & vibration tolerance

Less than 1 Error in 10^{14} bits read

W/E Endurance: 4,000,000 write/erase cycles

RoHS compliant

Part Numbering Information:

Unity Digital Part Number	Physical Capacity
UP128MS1xxxxxx	128MB
UP256MS1xxxxxx	256MB
UP512MS1xxxxxx	512MB
UP1GS1xxxxxx	1GB
UP2GS1xxxxxx	2GB
UP4GS1xxxxxx	4GB
UP8GS1xxxxxx	8GB

U	Form Factor	Capacity	Family	Chip Density
Name	PC Card	128MB~8GB	B: Bronze	2:512Mb
			S1: Silver	3: 1Gb
			G: Gold	4: 2Gb
				5: 4Gb
				6: 8Gb
				7: 16Gb

NAND Manufacturer	Programming Mode	Temperature
M: Micron	I: Fixed IDE	Blank: Commercial
S: Samsung	M: PC Card Memory	I: Industrial/I-Temp
T: Toshiba		
I: Intel		
Z: Spansion		

Environmental Characterization

Item	Performance
Temperature Cycle	JEDEC - JESD STD A104 Temp condition N (-40°C to 85 °C) and soak mode 3; 200 cycles
Humidity	MIL-STD 810F, Method 507.4, Paragraph 4.5.2 - 10 day test per figure 507.4-1, 10 day test
Vibration	MIL-STD 810F, Method 514.5, procedure 1, category 24, 1 hour per axis
Shock	MIL-STD 810F, Method 516.5, procedure 1, non-operational, 40g, SRS functional shock for ground equipment, three (3) shock per axis (positive or negative) JEDEC- JESD22-B, 104A, test condition B, 1500g pulse, 0.5 msec
Altitude	MIL-STD 810F, Method 500.4, procedure II, modified to 80,000 ft and non-operation 1 hr test duration at altitude.

Product Reliability

Item	Value
MTBF(@25°C)	> 4,000,000 Hours
Data Reliability	< 1 Non-Recoverable Error in 1014 Bits Read
Endurance	> 4,000,000 write/erase cycles

Product Performance*

Item	Performance (PIO mode 4 true IDE)
Read Transfer Rate	(Typical) Up to 8MB/s
Write Transfer Rate	(Typical) Up to 6MB/s
Burst Transfer Rate	Up to 16.7MB/s
Controller Overhead (Command to DRQ)	1ms typical, 5ms (max)

***Product performance will vary depending on application.**

DC Electrical Characteristics

Symbol	Parameter	Min	Max	Units	Notes
V_{IL}	Input LOW Voltage	-0.30	0.80	V	VCC= 5.0V
V_{IH}	Input HIGH Voltage	2.00	VCC+0.3	V	VCC= 5.0V
V_{OL}	Output LOW Voltage		0.45	V	VCC= 5.0V
V_{OH}	Output HIGH Voltage	2.40		V	VCC= 5.0V
I_{CC}	Operating Current, VCC_R=5.0V				
	Sleep Mode		0.20	mA	
	Operating Current		30.00	mA	
I_{CC}	Operating Current, VCC_R=3.3V				
	Sleep Mode		0.20	mA	
	Operating Current		30.00	mA	
I_{LI}	Input Leakage Current		±10	µA	
I_{LO}	Output Leakage Current		±10	µA	

PC Card Attribute Memory Read and Write AC Characteristics

VCC = 5V ± 0.5V, 3.3 V ± 0.3V

Symbol	Parameter	Min	Max	Units	Notes
t_{cR}	Read Cycle Time	250		ns	
$t_{a(A)}$	Address Access Time		250	ns	
$t_{a(CE)}$	Card Enable Access Time		250	ns	
$t_{a(OE)}$	Output Enable Access Time		125	ns	
$t_{dis(CE)}$	Output Disable time from CE		100	ns	
$t_{dis(OE)}$	Output Disable time from OE		100	ns	
$t_{en(CE)}$	Output Enable time from CE	5		ns	
$t_{en(OE)}$	Output Enable time from OE	5		ns	
$t_{V(A)}$	Data valid time from address change	0		ns	
$t_{su(A)}$	Address Setup Time	30		ns	
$t_{h(A)}$	Address Hold Time	20		ns	
$t_{su(CE)}$	Card Enable Setup Time	0		ns	
$t_{h(CE)}$	Card Enable Hold Time	20		ns	
t_{cW}	Write Cycle Time	250		ns	
$t_{w(WE)}$	Write Pulse Time	150		ns	
$t_{su(A-WEH)}$	Address setup time for WE	180		ns	
$t_{su(CE-WEH)}$	Card Enable setup time for WE	180		ns	
$t_{su(D-WEH)}$	Data setup time for WE	80		ns	
$t_{h(D)}$	Data hold time	30		ns	
$t_{dis(WE)}$	Output disable time from WE		100	ns	
$t_{en(WE)}$	Output enable time from WE	5		ns	
$t_{su(OE-WE)}$	Output Enable setup time for WE	10		ns	
$t_{h(OE-WE)}$	Output Enable hold time from WE	10		ns	

Common Memory Read and Write AC Characteristics

Symbol	Parameter	Min	Max	Units
t_{cR}	Read Cycle Time	150		ns
$t_{a(A)}$	Address Access Time		150	ns
$t_{a(CE)}$	Card Enable Access Time		150	ns
$t_{a(OE)}$	Output Enable Access Time		75	ns
$t_{dis(CE)}$	Output Disable time from CE		75	ns
$t_{dis(OE)}$	Output Disable time from OE		75	ns
$t_{en(CE)}$	Output Enable time from CE	5		ns
$t_{en(OE)}$	Output Enable time from OE	5		ns
$t_{V(A)}$	Data valid time from address change	0		ns
$t_{su(A)}$	Address Setup Time	20		ns
$t_{h(A)}$	Address Hold Time	20		ns
$t_{su(CE)}$	Card Enable Setup Time	0		ns
$t_{h(CE)}$	Card Enable Hold Time	20		ns
t_{cW}	Write Cycle Time	150		ns
$t_{w(WE)}$	Write Pulse Time	80		ns
$t_{su(A-WEH)}$	Address setup time for WE	100		ns
$t_{su(CE-WEH)}$	Card Enable setup time for WE	100		ns
$t_{su(D-WEH)}$	Data setup time for WE	50		ns
$t_{h(D)}$	Data hold time	20		ns
$t_{rec(WE)}$	Write recovery time	20		ns
$t_{dis(WE)}$	Output disable time from WE		75	ns
$t_{en(WE)}$	Output enable time from WE	5		ns
$t_{su(OE-WE)}$	Output Enable setup time for WE	10		ns
$t_{h(OE-WE)}$	Output Enable hold time from WE	10		ns

I/O Access Read and Write AC Characteristic

Symbol	Parameter	Min	Max	Units
$t_{d(IORD)}$	Data Delay after IORD		100	ns
$t_{h(IORD)}$	Data Hold following IORD	0		ns
$t_{w(IORD)}$	IORD pulse width	165		ns
$t_{suA(IORD)}$	Address setup time for IORD	70		ns
$t_{hA(IORD)}$	Address hold time for IORD	20		ns
$t_{suCE(IORD)}$	Card Enable setup time for IORD	5		ns
$t_{hCE(IORD)}$	Card Enable hold time from IORD	20		ns
$t_{suREG(IORD)}$	REG setup time for IORD	5		ns
$t_{hREG(IORD)}$	REG Hold time from IORD	0		ns
$t_{dfl\ NP(IORD)}$	INPACK delay falling from IORD	0	45	ns
$t_{drlNP(IORD)}$	INPACK delay rising from IORD		45	ns
$t_{dfl\ O16(IORD)}$	IOIS16 delay falling from address		35	ns
$t_{drlO16(IORD)}$	IOIS16 delay rising from address		35	ns
$t_{su(IOWR)}$	Data setup time for IOWR	60		ns
$t_{h(IOWR)}$	Data hold time from IOWR	30		ns
$t_{w(IOWR)}$	IOWR pulse width	165		ns
$t_{suA(IOWR)}$	Address setup time for IOWR	70		ns
$t_{hA(IOWR)}$	Address hold time from IOWR	20		ns
$t_{suCE(IOWR)}$	Card Enable setup time for IOWR	5		ns
$t_{hCE(IOWR)}$	Card Enable hold time from IOWR	20		ns
$t_{suREG(IOWR)}$	REG setup time for IOWR	5		ns
$t_{hREG(IOWR)}$	REG hold time from IOWR	0		ns

True-IDE Mode I/O Access Read and Write AC Characteristics

Symbol	Parameter	Min	Max	Units
t_{cR}	Cycle time	120		ns
t_{suA}	Address setup time for IORD/IOWR	25		ns
t_{hA}	Address hold time from IORD/IOWR	10		ns
t_{w}	IORD/IORW recovery time	70		ns
t_{rec}	IORD/IORW recovery time	25		ns
$t_{suD(IORD)}$	Data setup time for IORD	20		ns
$t_{hD(IORD)}$	Data hold time for IORD	5		ns
$t_{dis(IORD)}$	Output disable time from IORD		30	ns
$t_{suD(IOWR)}$	Data setup time for IOWR	20		ns
$t_{hD(IOWR)}$	Data hold following IOWR	10		ns

Pin Assignments & Pin Type

	PC Card Memory Mode			PC Card I/O Mode			True IDE Mode		
Pin No.	**Signal Name**	**Pin Type**	**I/O Type**	**Signal Name**	**Pin Type**	**I/O Type**	**Signal Name**	**Pin Type**	**I/O Type**
1	GND		Ground	GND		Ground	GND		Ground
2	D03	I/O	I1Z, OZ3	D03	I/O	I1Z, OZ3	D03	I/O	I1Z, OZ3
3	D04	I/O	I1Z, OZ3	D04	I/O	I1Z, OZ3	D04	I/O	I1Z, OZ3
4	D05	I/O	I1Z, OZ3	D05	I/O	I1Z, OZ3	D05	I/O	I1Z, OZ3
5	D06	I/O	I1Z, OZ3	D06	I/O	I1Z, OZ3	D06	I/O	I1Z, OZ3
6	D07	I/O	I1Z, OZ3	D07	I/O	I1Z, OZ3	D07	I/O	I1Z, OZ3
7	-CE1	I	I3U	-CE1	I	I3U	-CSO	I	I3U
8	A10	I	IZ1	A10	I	IZ1	A10[2]	I	IZ1
9	-OE	I	IU3	-OE	I	IU3	-ATA SEL	I	IU3
10	NC			NC			NC		
11	A09	I	I1Z	A09	I	I1Z	A09[2]	I	I1Z
12	A08	I	I1Z	A08	I	I1Z	A08[2]	I	I1Z
13	NC			NC			NC		
14	NC			NC			NC		
15	-WE	I	I3U	-WE	I	I3U			
16	RDY/BSY	O	OT1	IREQ	O	OT1	INTRQ	O	OT1
17	Vcc		Power	Vcc		Power	Vcc		Power
18	NC			NC			NC		
19	NC			NC			NC		
20	NC			NC			NC		
21	NC			NC			NC		
22	A07	I	I1Z	A07	I	I1Z	A07[2]	I	I1Z
23	A06	I	I1Z	A06	I	I1Z	A06[2]	I	I1Z
24	A05	I	I1Z	A05	I	I1Z	A05[2]	I	I1Z
25	A04	I	I1Z	A04	I	I1Z	A04[2]	I	I1Z
26	A03	I	I1Z	A03	I	I1Z	A03[2]	I	I1Z
27	A02	I	I1Z	A02	I	I1Z	A02	I	I1Z
28	A01	I	I1Z	A01	I	I1Z	A01	I	I1Z
29	A00	I	I1Z	A00	I	I1Z	A00	I	I1Z
30	D00	I/O	I1Z, OZ3	D00	I/O	I1Z, OZ3	D00	I/O	I1Z, OZ3
31	D01	I/O	I1Z, OZ3	D01	I/O	I1Z, OZ3	D01	I/O	I1Z, OZ3
32	D02	I/O	I1Z, OZ3	D02	I/O	I1Z, OZ3	D02	I/O	I1Z, OZ3
33	WP	O	OT3	-IOIS16	O	OT3	-IOCS16	O	ON3
34	GND		Ground	GND		Ground	GND		Ground
35	GND		Ground	GND		Ground	GND		Ground
36	-CD1	O	Ground	-CD1	O	Ground	-CD1	O	Ground
37	D11[1]	I/O	I1Z, OZ3	D11[1]	I/O	I1Z, OZ3	D11	I/O	I1Z, OZ3
38	D12[1]	I/O	I1Z, OZ3	D12[1]	I/O	I1Z, OZ3	D12	I/O	I1Z, OZ3
39	D13[1]	I/O	I1Z, OZ3	D13[1]	I/O	I1Z, OZ3	D13	I/O	I1Z, OZ3
40	D14[1]	I/O	I1Z, OZ3	D14[1]	I/O	I1Z, OZ3	D14	I/O	I1Z, OZ3
41	D15[1]	I	I1Z, OZ3	D15[1]	I	I1Z, OZ3	D15	I	I1Z, OZ3
42	-CE2[1]	I	I3U	-CE2[1]	I	I3U	-CS1	I	I3U
43	VS1	O	Ground	VS1	O	Ground	VS1	O	Ground
44	-IORD	I	I3U	-IORD	I	I3U	-IORD	I	I3U
45	-IOWR	I	I3U	-IOWR	I	I3U	-IOWR	I	I3U
46	NC			NC			NC		
47	NC			NC			NC		
48	NC			NC			NC		
49	NC			NC			NC		
50	NC			NC			NC		
51	Vcc		Power	Vcc		Power	Vcc		Power
52	NC			NC			NC		
53	NC			NC			NC		
54	NC			NC			NC		
55	NC			NC			NC		
56	-CSEL	I	I2Z	-CSEL	I	I2Z	-CSEL	I	I2Z
57	VS2	O	Open	VS2	O	Open	VS2	O	Open
58	RESET	I	I2Z	RESET	I	I2Z	-RESET	I	I2Z
59	-Wait	O	OT1	-Wait	O	OT1	IORDY	O	ON1
60	-INPACK	O	OT1	-INPACK	O	OT1	DMARQ	O	OT1
61	-REG	I	I3U	-REG	I	I3U	-DMACK	I	I3U
62	BVD2	I/O	OT1	-SPKR	I/O	OT1	DASP	I/O	ITU, ON1
63	BVD1	I/O	OT1	-STSCHG	I/O	OT1	-PDIAG	I/O	ITU, ON1
64	D08[1]	I/O	I1Z, OZ3	D08[1]	I/O	I1Z, OZ3	D08[1]	I/O	I1Z, OZ3
65	D09[1]	I/O	I1Z, OZ3	D09[1]	I/O	I1Z, OZ3	D09[1]	I/O	I1Z, OZ3
66	D10[1]	O	OZ3	D10[1]	O	OZ3	D10[1]	O	OZ3
67	-CD2	O	Ground	-CD2	O	Ground	-CD2	O	Ground
68	GND		Ground	GND		Ground	GND		Ground

Note:

[1] These signals are required only for 16-bit access and are not required when installed in 8-bit systems. Devices should allow for 3-state signals not to consume current.

[2] Should be grounded by the host system.

[3] Should be tied to VCC by the host system.

[4] The -CSEL signal is ignored by the drive in PC Card modes. However, because it is not pulled up on the drive in these modes, it should not be left floating by the host in PC Card modes; the pin should be connected by the host to PC Card A25 or grounded by the host.

[5] If DMA operations are not used, the signal should be held high or tied to VCC by the host. For proper operation in older hosts, while DMA operations are not active, the drive shall ignore the signal, including a floating condition.

Signal Description

Signal Name	Dir.	Pin	Description
A10-A0 (PC Card Memory Mode)	I	8, 11,12,,22, 23, 24, 25, 26, 27, 28, 29	These address lines along with the -REG signal are used to select the following: The I/O port address registers within the storage card, the memory mapped port address registers within the storage card, a byte in the drive's information structure and its configuration control and status registers.
A10-A0 (PC Card I/O Mode)			This signal is the same as the PC Card Memory Mode signal.
A2 - A0 (True IDE Mode)		27, 28, 29	In True IDE Mode, only A[2:0] are used to select the one of eight registers in the Task File, the remaining address lines should be grounded by the host.
BVD1 (PC Card Memory Mode)	I/O	63	This signal is asserted high, as BVD1 is not supported.
-STSCHG (PC Card I/O Mode) Status Changed			This signal is asserted low to alert the host to changes in the READY and Write Protect states, while the I/O interface is configured. Its use is controlled by the Card Config and Status Register.
-PDIAG (True IDE Mode)			In the True IDE Mode, this input / output is the Pass Diagnostic signal in the Master / Slave handshake protocol.
BVD2 (PC Card Memory Mode)	I/O	62	This signal is asserted high, as BVD2 is not supported.
-SPKR (PC Card I/O Mode)			This line is the Binary Audio output from the drive. If the drive does not support the Binary Audio function, this line should be held negated.
-DASP (True IDE Mode)			In the True IDE Mode, this input/output is the Disk Active/Slave Present signal in the Master/Slave handshake protocol.
-CD1, -CD2 (PC Card Memory Mode)	O	36, 67	These Card Detect pins are connected to ground on the storage card. They are used by the host to determine that the storage card is fully inserted into its socket.
-CD1, -CD2 (PC Card I/O Mode)			This signal is the same for all modes.
-CD1, -CD2 (True IDE Mode)			This signal is the same for all modes.
-CE1, -CE2 (PC Card Memory Mode) Card Enable	I	7, 42	These input signals are used both to select the drive and to indicate to the drive whether a byte or a word operation is being performed. -CE2 always accesses the odd byte of the word. -CE1 accesses the even byte or the Odd byte of the word depending on A0 and -CE2. A multiplexing scheme based on A0, -CE1, -CE2 allows 8-bit hosts to access all data on D0-D7.
-CE1, -CE2 (PC Card I/O Mode) Card Enable			This signal is the same as the PC Card Memory Mode signal.
-CS0, CS1 (True IDE Mode)			In the True IDE Mode, -CS0 is the chip select for the task file registers while -CS1 is used to select the Alternative Status Register and the Device Control Register. While -DMACK is asserted, -CS0 and -CS1 shall be held negated and the width of the transfers shall be 16 bits.
-CSEL (PC Card Memory Mode)	I	56	This signal is not used for this mode, but should be connected by the host to PC Card A25 or grounded by the host.
-CSEL (PC Card I/O Mode)			This signal is not used for this mode, but should be connected by the host to PC Card A25 or grounded by the host.
-CSEL (True IDE Mode)			This internally pulled up signal is used to configure this device as a Master or a Slave when configured in the True IDE Mode. When this pin is grounded, this device is configured as a Master. When the pin is open, this device is configured as a Slave.

Signal Name	Dir.	Pin	Description
D15 - D00 (PC Card Memory Mode)	I/O	2, 3, 4, 5, 6, 30, 31, 32, 37, 38, 39, 40, 41, 64, 65, 66	These lines carry the Data, Commands and Status information between the host and the controller . D00 is the LSB of the Even Byte of the Word. D08 is the LSB of the Odd Byte of the Word.
D15 - D00 (PC Card I/O Mode)			This signal is the same as the PC Card Memory Mode signal.
D15 - D00 (True IDE Mode)			In True IDE Mode, all Task File operations occur in byte mode on the low order bus D[7:0] while all data transfers are 16 bit using D[15:0].
GND (PC Card Memory Mode)	-	1, 34, 35, 68	Ground
GND (PC Card I/O Mode)			The signal is the same for all modes
GND (True IDE Mode)			The signal is the same for all modes
-INPACK (PC Card Memory Mode)	O	60	This signal is the same for all modes
-INPACK (PC Card I/O Mode) Input Acknowledge			The input Acknowledge signal is asserted by the storage drive or CF drive when the drive is selected and responding to an I/O read cycle at the address that is on the address bus. This signal is used by the host to control the enable of any input data buffers between the storage drive or CF drive and the CPU.
DMARQ (True IDE Mode)			This signal is a DMA Request that is used for DMA data transfers between host and device. It shall be asserted by the device when it is ready to transfer data to or from the host. For Multiword DMA transfers, the direction of data transfer is controlled by -DIOR and -DIOW. This signal is used in a handshake manner with -DMACK, i.e., the device shall wait until the host asserts -DMACK before negating DMARQ, and re asserting DMARQ if there is more data to transfer. While a DMA operation is in progress, -CS0 and -CS1 shall be held negated and the width of the transfers shall be 16 bits. If there is no hardware support for DMA mode in the host, this output signal is not used and should not be connected at the host. In this case, the BIOS must report that DMA mode is not supported by the host so that device drivers will not attempt DMA mode. A host that does not support DMA mode and implements both PCMCIA and True IDE modes of operation need not alter the PCMCIA mode connections while in True IDE mode as long as this does not prevent proper operation in any mode.
-IORD (PC Card Memory Mode)	I	44	This signal is not used in this mode
-IORD (PC Card I/O Mode)			This is an I/O strobe generated by the host. This signal gates I/O data onto the bus from the storage drive or CF drive when the drive is configured to use the I/O interface
-IORD (True IDE Mode)			In True IDE Mode, this signal has the same function as in PC Card I/O Mode.

Signal Name	Dir.	Pin	Description
-IOWR (PC Card Memory Mode)	I	45	This signal is not used in this mode
-IOWR (PC Card I/O Mode)			The I/O Write strobe pulse is used to clock I/O data on the Card Data bus into the storage card or CF Drive controller registers when the storage drive or CF drive is configured to use the I/O interface. The clocking shall occur on the negative to positive edge of the signal (trailing edge).
-IOWR (True IDE Mode)			In True IDE Mode, this signal has the same function as in PC Card I/O Mode.
-OE (PC Card Memory Mode)	I	9	This is an Output Enable strobe generated by the host interface. It is used to read data from the storage card or CF drive in Memory Mode and to read the CIS and configuration registers.
-OE (PC Card I/O Mode)			In PC Card I/O Mode, this signal is used to read the CIS and configuration registers.
-ATA SEL (True IDE Mode)			To enable True IDE Mode this input should be grounded by the host.
Ready (PC Card Memory Mode)	O	16	In Memory Mode, this signal is set high when the storage card or CF drive is ready to accept a new data transfer operation and is held low when the drive is busy. At power up and at Reset, the READY signal is held low (busy) until the storage card or CF drive has completed its power up or reset function. No access of any type should be made to the storage card or CF drive during this time. Note, however, that when a drive is powered up and used with RESET continuously disconnected or asserted, the Reset function of the RESET pin is disabled. Consequently, the continuous assertion of RESET from the application of power shall not cause the READY signal to remain continuously in the busy state.
-IREQ (PC Card I/O Mode)			I/O Operation – After the storage drive or CF drive has been configured for I/O operation, this signal is used as -Interrupt Request. This line is strobed low to generate a pulse mode interrupt or held low for a level mode interrupt.
INTRQ			In True IDE Mode signal is the active high Interrupt Request to the host.
-REG (PC Card Memory Mode)	I	61	This signal is used during Memory Cycles to distinguish between Common Memory and Register (Attribute) Memory accesses. High for Common Memory, Low for Attribute Memory.
-REG (PC Card I/O Mode)			The signal shall also be active (low) during I/O Cycles when the I/O address is on the Bus.
-DMACK (True IDE Mode)			This is a DMA Acknowledge signal that is asserted by the host in response to DMARQ to initiate DMA transfers. While DMA operations are not active, the drive shall ignore the -DMACK signal, including a floating condition. If DMA operation is not supported by a True IDE Mode only host, this signal should be driven high or connected to VCC by the host. A host that does not support DMA mode and implements both PCMCIA and True IDE modes of operation need not alter the PCMCIA mode connections while in True IDE mode as long as this does not prevent proper operation all modes.

Signal Name	Dir.	Pin	Description
RESET (PC Card Memory Mode)	I	58	The storage card is Reset when the RESET pin is high with the following important exception: The host may leave the RESET pin open or keep it continually high from the application of power without causing a continuous Reset of the card. Under either of these conditions, the card shall emerge from power-up having completed an initial Reset. The storage card is also Reset when the Soft Reset bit in the Card Configuration Option Register is set.
RESET (PC Card I/O Mode)			This signal is the same as the PC Card Memory Mode signal.
-RESET (True IDE Mode)			In the True IDE Mode, this input pin is the active low hardware reset from the host.
VCC (PC Card Memory Mode)	-	17, 51	+5 V, +3.3 V power.
VCC (PC Card I/O Mode)			This signal is the same for all modes.
VCC (True IDE Mode)			This signal is the same for all modes.
-VS1 **-VS2 (PC Card Memory Mode**	O	43, 57	Voltage Sense Signals. -VS1 is grounded on the Card and sensed by the Host so that the storage card CIS can be read at 3.3 volts and -VS2 is reserved by PCMCIA for a secondary voltage and is not connected on the Card.
-VS1 **-VS2 (PC Card I/O Mode)**			This signal is the same for all modes.
-VS1 **-VS2 (True IDE Mode)**			This signal is the same for all modes.
-WAIT (PC Card Memory Mode)	O	59	The -WAIT signal is driven low by the storage card to signal the host to delay completion of a memory or I/O cycle that is in progress.
-WAIT (PC Card I/O Mode)			This signal is the same as the PC Card Memory Mode signal.
IORDY (True IDE Mode)			In True IDE Mode, this output signal may be used as IORDY.
-WE (PC Card Memory Mode)	I	15	This is a signal driven by the host and used for strobing memory write data to the registers of the storage card when the card is configured in the memory interface mode. It is also used for writing the configuration registers.
-WE (PC Card I/O Mode)			In PC Card I/O Mode, this signal is used for writing the configuration registers.
-WE (True IDE Mode)			In True IDE Mode, this input signal is not used and should be connected to VCC by the host.
WP (PC Card Memory Mode)	O	33	Memory Mode – storage card does not have a write protect switch. This signal is held low after the completion of the reset initialization sequence.
-IOIS16 (PC Card I/O Mode)			I/O Operation – When the storage card is configured for I/O Operation Pin 24 is used for the -I/O Selected is 16 Bit Port (-IOIS16) function. A Low signal indicates that a 16 bit or odd byte only operation can be performed at the addressed port.
-IOCS16 (True IDE Mode)			In True IDE Mode this output signal is asserted low when this device is expecting a word data transfer cycle.

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